CPC1310

Embedded COM Express Basic module

User Manual

Rev. 0.05
March 2014

The product described in this manual is compliant with all related CE standards.

Product Title: CPC1310
Document name: CPC1310 User Manual
Manual version: 0.05

Revision Record

Revision No.	Brief description of changes	Board index	Revision date
0.01	Initial version	CPC1310	November 2012
0.02	Changes in Phoenix® BIOS section	CPC1310	December 2012
0.03	Clarification of drawing dimensions	CPC1310	December 2012
0.04	Subsection 6.3. contains recommendations for ensuring galvanic insulation	CPC1310	January 2013
0.05	For GPI (0-3) signals in Table 5-1, the following note was made: “Pull-up 5k+16.5k to 3.3V”	CPC1310	February 2013

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TRANSPORTATION, UNPACKING AND STORAGE

Transportation

The device should be transported in original manufacturer's separate packaging (transport packaging), which contains an individual antistatic bag and a cardboard box, in the closed transport (automobile, railway, air transportation in heated and pressurized compartments) in storage conditions 5 defined in the IEC 721-2-1 standard (GOST standard 15150-69) or in storage conditions 3 during sea transportation.

The packaged modules should be transported in accordance with the shipping rules, specified for this particular type of transport.

During handling and transportation operations, the packaged modules should not undergo sharp pounding, falls, shocks and exposure to atmospheric precipitation. The goods should be stored in a carrier vehicle in such a manner which will prevent their moving.

Unpacking

Prior to unpacking, before transportation at subzero temperature of ambient air the modules should be kept within 6 hours under storage conditions 1 defined in the IEC 721-2-1 standard (GOST standard 15150-69).

It is prohibited to place the packaged module close to the heat source, prior to unpacking.

Retain all original packaging at least until the warranty period is over. You may need it for shipments or for storage of the product.

After unpacking the product, you should inspect it for visible damage that could have occurred during shipping or unpacking. If damage is observed (usually in the form of bent component leads or loose socketed components), contact Fastwel's official distributor from which you have purchased the product for additional instructions.

Storage

Module storage conditions for group 1 are defined in the IEC 721-2-1 standard (GOST standard 15150-69).

MANUFACTURER'S WARRANTY

Warranty Liabilities

The Manufacturer hereby guarantees the product conformity with the requirements of the 4013- 025-72782511-09 technical conditions provided that the Consumer complies with the operating, storage, transportation and installation conditions and procedures, specified by the accompanying documents.
The Manufacturer hereby guarantees that the products supplied thereby are free from defects in workmanship and materials, provided operation and maintenance norms were observed during the currently established warranty period. The Manufacturer's obligation under this warranty is to repair or replace free of charge any defective electronic component being a part of a returned product.
Products that broke down through the Manufacturer's fault during the warranty period will be repaired free of charge. Otherwise the Consumer will be invoiced as per the current labor remuneration rates and expendable materials cost

Liability Limitation Right

The Manufacturer shall not be liable for the damage inflicted to the Consumer's property because of the product breakdown in the process of its utilization.

Warranty Period

The warranty period for the products made by Fastwel Group is 24 months since the sale date (unless otherwise provided by the supply contract).
The warranty period for the custom-made products is 36 months since the sale date (unless otherwise provided by the supply contract.

Limitation of warranty liabilities

The above warranty liabilities shall not be applied:
To the products (including software), which were repaired or were amended by the employees, that do not represent the manufacturer. Exceptions are the cases where the customer has made repairs or made amendments to the devices in the strict compliance with instructions, preliminary agreed and approved by the manufacturer in writing;
To the products, broken down due to unacceptable polarity reversal (to the opposite sign) of the power supply, improper operation, transportation, storage, installation, mounting or accident.

Returning a product for repair

1. Apply to Fastwel company or to any of the Fastwel's official representatives for the Product Return Authorization.
2. Attach a failure inspection report with a product to be returned in the form, accepted by the Manufacturer, with a description of the failure circumstances and symptoms.
3. Place the product in the consumer packaging (antistatic bag) and cardboard box, in which the product had been supplied. Failure to package in antistatic material will VOID all warranties of the Customer on a unilateral basis.
4. The customer pays for shipping the product to Fastwel or to an official Fastwel representative or dealer

1. Introduction

1.1. Purpose

CPC1310 is designed in COM Express standard (PICMG COM.0 r.2.0) and is based on Intel Atom N450/ D510 CPUs, operating at the frequencies up to 1,66 GHz, and is used for embedded applications requiring high performance and low power consumption.
The module has 2x Serial ATA ports, 4x PCI Express ports x1, 8x USB ports, LPC, LVDS (18 bit), NAND Flash, two Ethernet channels, ISA interface.
KIB1283 or KIB1280 (with limited functionalities) boards will be used as carrier boards.
Module is supplied with installed FreeDOS operating system (hereinafter referred to as the Operating System or OS) and is compatible with the following operating systems: QNX 6.5, Windows XP (embedded), Linux 2.6.
User Manual contains information on correct and safe installation procedure, start and configuration of the module, connection and interaction with KIB1283 carrier board. It also covers issues related to start, debugging, and operation of the module as well as use of programs from among the basic and utility software (hereinafter referred to as the software).

1.2. Versions, ordering information

Module's versions and their part numbers (ordering information) are given in the table and shown on the figure below:

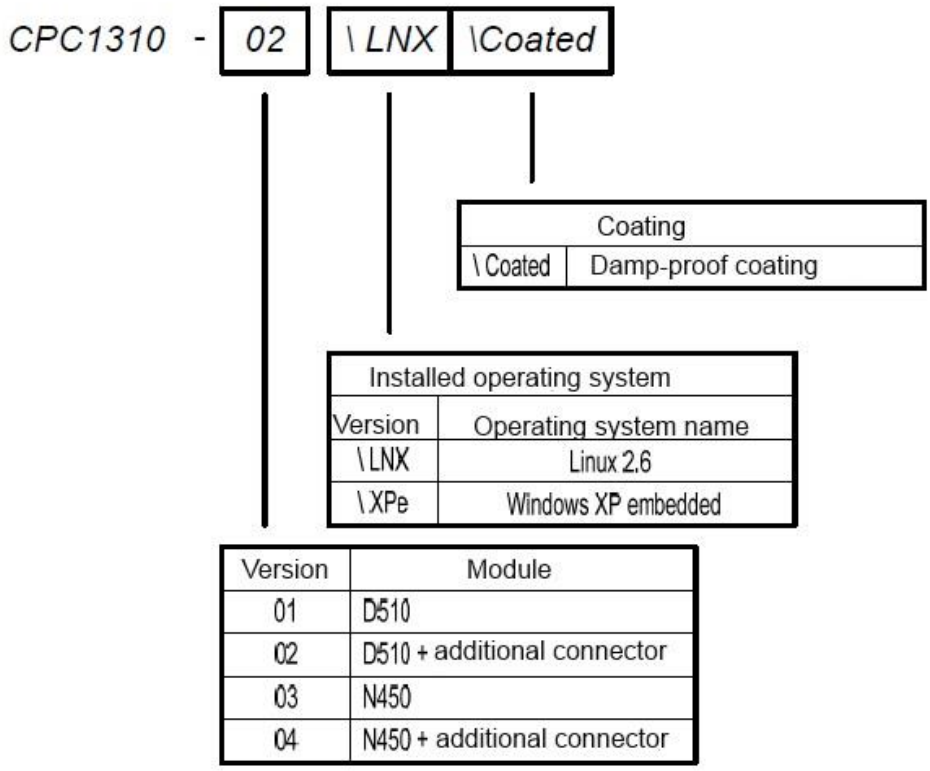
Tab. 1-1: Ordering information

Name	Product name	Part number	Description
CPU module CPC1310	CPC1310	CPC1310-01[1]	Intel Atom Pineview-D (D510) CPU COM Express basic TYPE II, 1 GB DDR-2 RAM
		CPC1310-02[2]	Intel Atom Pineview-D (D510) CPU COM Express basic TYPE II with extension (ISA, additional 1 Gb LAN), 1 GB DDR-2 RAM
		CPC1310-03[3]	Intel Atom Pineview-M (N450) CPU COM Express basic TYPE II, 1 GB DDR-2 RAM
		CPC1310-04[4]	Intel Atom Pineview-M (N450) CPU COM Express basic TYPE II with extension (ISA, additional 1 Gb LAN), 1 GB DDR-2 RAM
		CPC1310-xx/LNX	Module's option with preinstalled Linux 2.6
		CPC1310-xx/XPe	Module's option with preinstalled Windows XP
		CPC1310-xx/yy/Coated	Coated version

1) Module contains a full set of integrated interfaces and functional units
2) Unlike CPC1310-01, this version is added with 1 Gb LAN, ISA interface and 8x digital I/O lines
3) Unlike CPC1310-01, this version has a single-core Intel Atom Pineview N450 CPU
4) Unlike CPC1310-03, this version is added with 1 Gb LAN, ISA interface and 8x digital I/O lines

Where xx – module's version (01, 02, 03, 04);
Where yy – option of the preinstalled OS (LNX, XPe).

Fig. 1-1: CPC1310 engineering sample



Ordering information example:
“CPU Module CPC1310-02\LNX”

Interpretation:
– COM Express, CPU Intel Pineview-M D510, 1.66 GHz, 1 MB Cash, 667 MHz FSB;
– Industrial temperature range: - 40°C to +70°C);
– DDR2 SDRAM 667 MHz without ECC 1 GB, soldered;
– Additional connector (ISA bus, second Ethernet channel, 8 bit GPIO);
– Preinstalled Linux 2.6.

Key features of CPC1310 versions are given in the table below:

Table 1-2: Key features of CPC1310 versions

Item No.	**Version**	**Key features**	
		ISA, LAN2	**CPU**
1	CPC1310-01	-	(Pineview-D) Atom D510
2	CPC1310-02	+	(Pineview-D) Atom D510
3	CPC1310-03	-	(Pineview-D) Atom N450
4	CPC1310-04	+	(Pineview-D) Atom N450

1.3. Delivery checklist

The delivery checklist for all the module versions is specified in the table below:

Table 1-3: Delivery checklist

Part number	Description
CPC1310-01 CPC1310-02 CPC1310-03 CPC1310-04	CPC1310 CPU Module
-	Installation kit
-	Package

1.3.1. Additional accessories

Additional accessories are specified in the table below:

Table 1-4: Additional accessories

Part number	Description
ACS30066	Heat sink and kit of mounting screws

ACS30066 kit is ordered as an option.

1.3.2. Carrier-board for CPC1310

CPC1310 module is installed into Fastwel KIB1283 carrier-board; KIB1280 carrier-board (with limited functionality) can also be used.
The carrier-boards are to be purchased separately.

2. Technical characteristics

2.1. Technical specifications

Technical specifications of CPC1310 are given in the table:

Table 2-1: Technical specifications of CPC1310

Technical specifications	Description
CPU Intel Pineview-M (-D) 1,66 GHz *	- D510 – Dual Core (CPC1310-01, CPC1310-02); N450 – Single Core (CPC1310-03, CPC1310-04); - IA 32-bit & 64-bit Technology; - Intel SIMD2 & 3 (SSE2 + SSE3 + SSSE3); - Hyperthreading Technology (2 threads); - L1 cache: 32 KB instructions, 24 KB data; - L2 cache: 512 KB (N450), 1 MB (D510); - Intel SpeedStep Technology (CPC1310-03, CPC1310-04).
RAM	- DDR2 SDRAM 667 MHz without ECC 1 GB, soldered.
Video output	- VGA interface is routed to connector with A, B connector rows (resolution up to 1400x1050 60 Hz for N450 and 2048x1536 60 Hz for D510); - LVDS interface is routed to connector with A, B connector rows (resolution up to 1280x800 60 Hz for N450 and 1366x768 60 Hz for D510, single-channel mode 18 bit)
PCI bus	Routed to the connector with C, D rows; Support of specification v.2.3 32-bit /33 MHz; Support of up to 4x bus master devices (CPC1310-01, CPC1310-03).
ISA bus (CPC1310-02, CPC1310-0):	- Routed to the additional connector; - 16 bit/8 MHz; - Support of DDMA, ISA IRQ.
LPC bus	-Routed to the connector with A, B rows; - Compatibility with specification 1.0; - Support of 2x Master/DMA devices
PCI-E bus	- Routed to the connector with A, B rows; - Compatible with specification PCI-E 1.1; - Support up to 4x devices in x1 mode (2,5 Gb/s)
SMBUS	- Compatibility with specification 2.0 - Speed up to 100 Kb/s; - Routed to the connector with A,B rows.

*) Sleep Mode is not supported by this CPU version.

FLASH BIOS	16 Mb SPI-Flash
FLASH-drive	- 4GB NAND Flash (2xchannels) connected to SATA interface: (50 MB/s read, 45 MB/s write). -
IDE interface	- 1xchannel - Support of ULTRA ATA/100 mode
SATA interface	- Transfer speed up to 300 MB/s - 2xchannels
Ethernet port	- Transfer speed up to 1000 MB/s, routed to the connector with A, B rows. - Transfer speed up to 1000 MB/s, routed to additional connector (CPC1310-02, CPC1310-04)
I2C interface	- Routed to the connector with A,B rows
USB port	- Support of USB 1.1 (12 Mb/s), USB 2.0 (480 Mb/s) - Connection of up to 8 x devices; - Routed to the connector with A, B rows
Digital I/O port	- 8 x programmable I/O lines, routed to the connector with A, B rows - 8 x programmable I/O lines, routed to the additional connector (CPC1310-02, CPC1310-04)
FRAM memory	- 64 Kb, RAM 256 byte for storing BIOS Setup settings; - Implemented on SMBUS
RTC	- Fed from lithium battery CR2032 (3V).
Audio support	- HD Audio digital interface - Routed to the connector with A,B rows.
2 x watchdog timers	- WDT1 with a fixed actuating range - WDT2 with programmed actuating range.
Hardware monitor	- Implemented on SMBUS - Monitoring of 3 supply voltages - Monitoring of CPU temperature - Monitoring of PCB temperature
Supported OS	- FreeDOS - Windows XP (embedded) - Linux 2.6. - QNX 6,5

2.2. Supply and consumption current

Supply of CPC1310 can be carried out in two modes and should correspond to the requirements of PICMG COM.0 r.2.0 standard.

Table 2-2: Operating mode and consumption current

Mode	Input voltage
Supply from ATX source, corresponding to specification r2.2 (using PS_ON# signal)	+11,4 to +12,6
	4,75 to +5,25
Extended range of input voltage*	+4,75 to +14
*) With the extended range of input voltage the consumption current will be as follows: - Supply voltage +5 V: no more than 2.9 A (CPC1310-01, -02) and 2.3 A (CPC1310-03, -04); - Supply voltage +5 V_STBY V: no more than 0,2 A (for all the versions of CPC1310); - Supply voltage +12 V: no more than 1,25 A (CPC1310-01, -02) and 1,1 A (CPC1310-03, -04).	

Note
Excluding the connected external devices, the power consumed by CPC1310 is no more than 15 W.

2.3 Resistance to climatic effects

CPC1310 modules are resistant to changes of ambient temperatures in the range from - 40 to + 70°C, with relative humidity of up to 80% without moisture condensation, in accordance with IEC 68-2-14-84.
The specified upper limit temperature value of operating range for CPC1310 is determined for module's operation without additional cooler. If you need to apply the module at temperatures of up to + 85°C it is necessary to use the ACS30066 kit (heat sink), which can be purchased as option. It is allowed to use heat-sink manufactured by the user and corresponding to cooling requirements of CPC1310 (see Annex A Recommendations for development of cooling devices).
CPC1310 modules are resistant to cyclic damp heat at the ambient temperature of + (55 ± 2)°C, relative humidity (93 ± 3)% (for conformal coating versions) in accordance with IEC 68-2-30-82.

2.4. Resistance to mechanical stress

The modules are resistant to sinusoidal vibrations for frequencies from 10 to 500 Hz with acceleration of 2g in accordance with IEC 68-2-6-82.

The modules are resistant to single shocks with a peak acceleration of 50 g, in accordance with IEC 68-2-27-87).

The modules are resistant to multiple shocks with a peak acceleration of 25 g, with 1000 shocks, in accordance with IEC 68-2-29-87.

2.5. Module dimensions

Mass and overall dimensions' values for module versions are specified in the table below.

Table 2-3: Weight and overall dimensions of the module

Module	Weight (in kg), no more than	Packed weight (in kg)	Overall dimensions with heat-spreader and stand-offs (mm), no more than	Package dimensions (in mm)
CPC1310	0,4	0,5	125,25 x 95,25 × 25	140 × 150 × 45

Overall and connection dimensions of the module are shown on the figures below.

2.6. MTBF

Mean time between failures (MTBF) for the ambient temperature of +30ºC corresponds to the value in table.

Table 2-4: MTBF

Module type	MTBF (in hours) is no less than
CPC1310	180000
Note – MTBF values are calculated using Telcordia Issue 1 calculation model (Method I Case 3) for continuous operation when located on land and under conditions corresponding to the Moderately Cold Climate 4 climatic category according to IEC 721-2-1:1982, at the ambient temperature of +30°C	

Fig. 2-1: Overall and connection dimensions of module (top view)

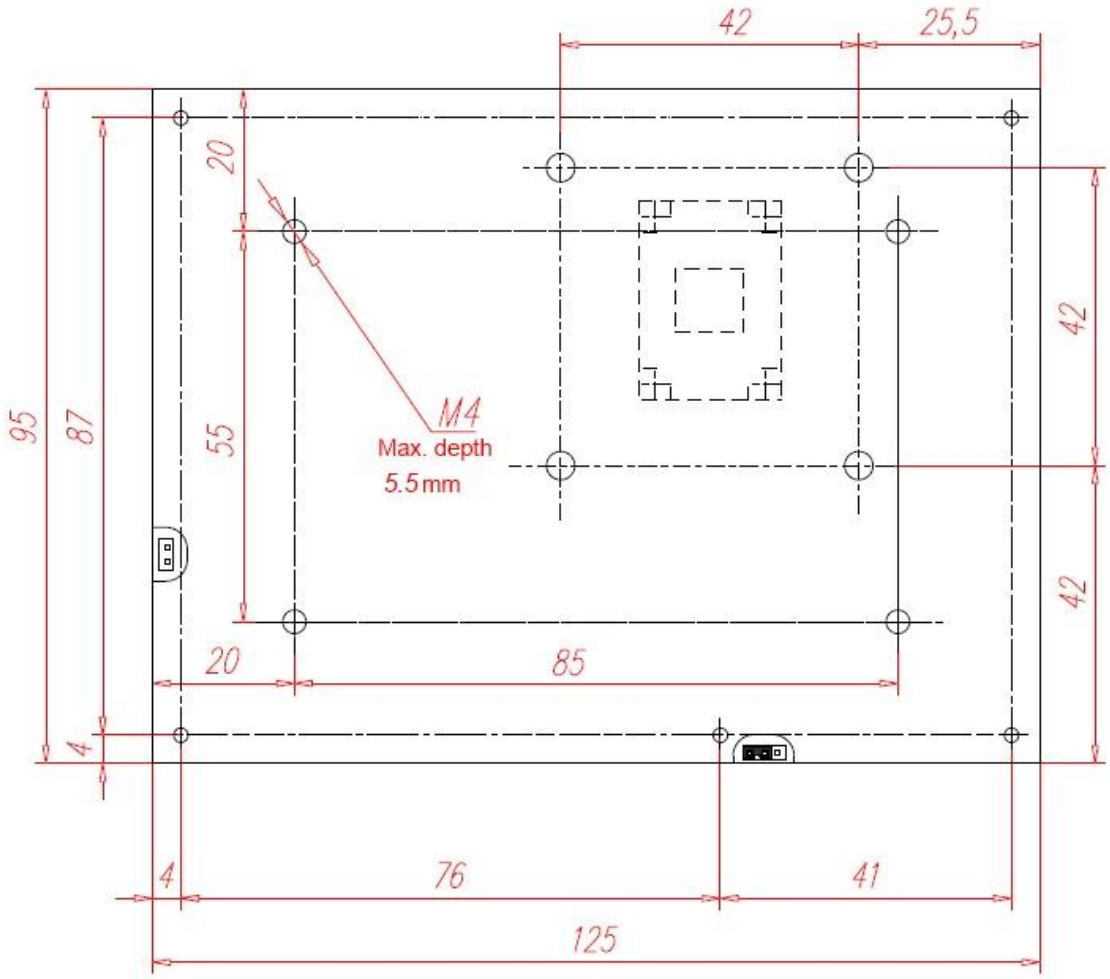
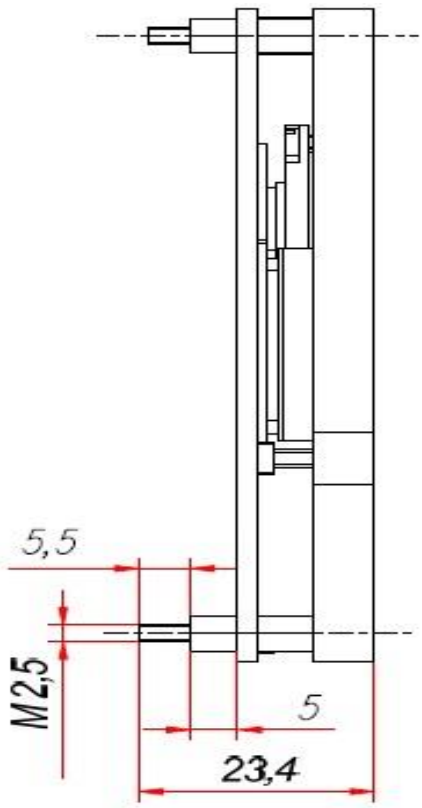


Fig. 2-2: Overall module's dimensions (side view)

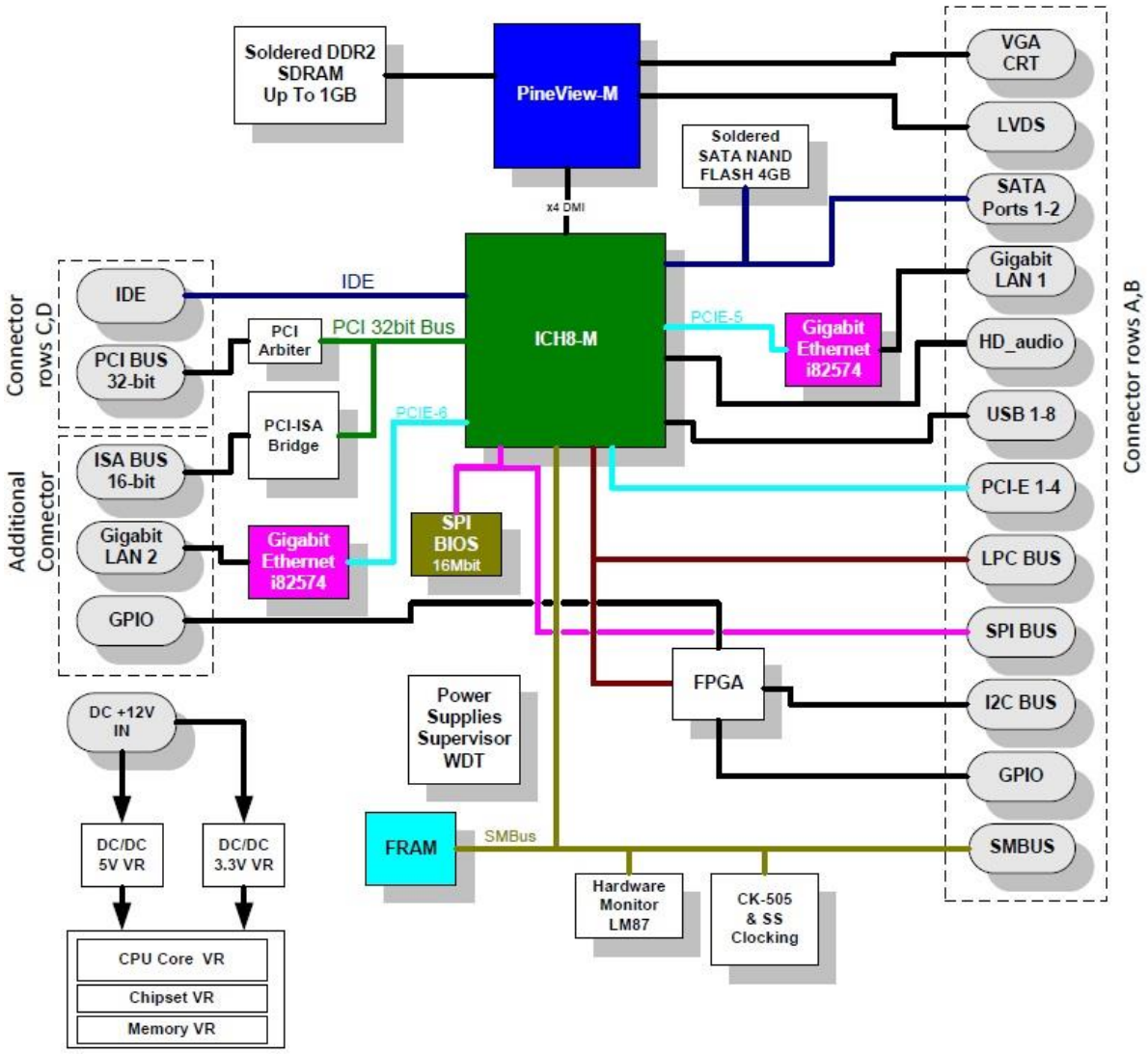


3. SPECIFICATION

3.1. Functional structure

The block diagram of the board is shown on the Figure:

Fig. 3-1: Block diagram of the board



Block diagram of the board shows its main functional units:

- CPU: Intel Pineview-M or Pineview-D (depending on the version);
- Chipset: Intel ICH8M;
- RAM DDR2 SDRAM (up to 1 GB);
- Flash BIOS (16 Mb);

- NAND Flash-drive (4 GB);
- VGA port (COM Express A-B connector);
- Port for the connection of LVDS-panel (COM Express A-B connector);
- 2 SATA channels (COM Express A-B connector);
- IDE interface for the connection Compact Flash or HDD (COM Express C-D connector);
- 2x independent Ethernet channels 10/100/1000 Mb/s (COM Express A-B connector and an additional connector);
- 8x USB 2.0 channels (COM Express A-B connector);
- LPC bus (COM Express A-B connector);
- 2x digital I/O ports (COM Express A-B connector and an additional connector);
- 4x PCI-E channels x1 (COM Express A-B connector);
- SMbus;
- I2C bus;
- Interface for the connection of HD Audio controller;
- ISA bus 16-bit (additional connector);
- PCI bus 32-bit 33 MHz (COM Express C-D connector);
- FRAM with serial interface (for saving the system configuration);
- 2x watchdog timers (WDT).

Brief description of the board's main functional units is given below:

CPU Intel Pineview-M (N450) or Intel Pineview-D (D510):
- 1x 32-/64- bit x86 core (N450);
- 2x 32-/64-bit x86 cores (D510);
- Support of SSE2, SSE3, SSSE2;
- Hyperthreading support;
- 64-bit memory bus;
- Level 1 (L1) cash – 32 KB program region, 24 KB data region;
- Level 2 (L2) cash – 512 KB (for N450);
- Level 2 (L2) cash – 1 MB (for D510);
- Support of Intel SpeedStep technology (for N450).
- RAM: DDR2 SDRAM 667 MHz (soldered) – 1 GB.
- Flash BIOS:
- 16 Mb;
- Modifiable in the system.
- 2x interfaces for the connection of Serial ATA drives (via KIB1283 carrier board).
- IDE interface for the connection of Compact Flash drives or ATA storage drive (via KIB1283 carrier board).
- NAND Flash storage device (soldered and connected to SATA interface) - 4 GB.
- Video controller:
- 2D/3D accelerator;
- Video memory capacity (assigned from system memory) is no more than 256 MB;

- Possibility to connect LCD panels (18-bit LVDS panels) with resolution up to no more than 1280 × 800 (60 Hz) and VGA monitors with resolution up to no more than 1400 × 1050 (60 Hz);
- Possibility to connect LCD panels (18-bit LVDS) with resolution up to no more than 1366 × 768 (60 Hz) and VGA monitors with resolution up to no more than 2048 × 1536 (60 Hz).
- 2x Ethernet controllers 10/100/1000 Mb/s.
- 4x PCI-E x1 ports (via KIB1283 carrier board):
- Support of PCI Express r1.1 specification.
- PCI interface (via KIB1283 carrier board):
- Support of PCI Local Bus r2.3 specification for 33 MHz bus.
- USB ports (via KIB1283 carrier board):
- Connection up to 8 devices;
- Support of USB 1.1 and 2.0 specifications;
- Support of OS boot from USB flash drive.
- LPC interface for the connection of I/O controller (Super I/O).
- HD Audio interface for the connection of audio controller.
- 2x I/O ports (via KIB1283 carrier board):
- 8x separately programmed I/O lines.
- I2C interface (via KIB1283 carrier board).
- SMBus interface (via KIB1283 carrier board).

3.2. Location of main components

Location of the components, connectors and switch panels for top and bottom views are shown on Fig. 3-2 and Fig. 3-3 accordingly.

Location of switches based on functions is demonstrated in Section 7 Configuration.

Fig. 3-2: Location of connectors and main components (top view)

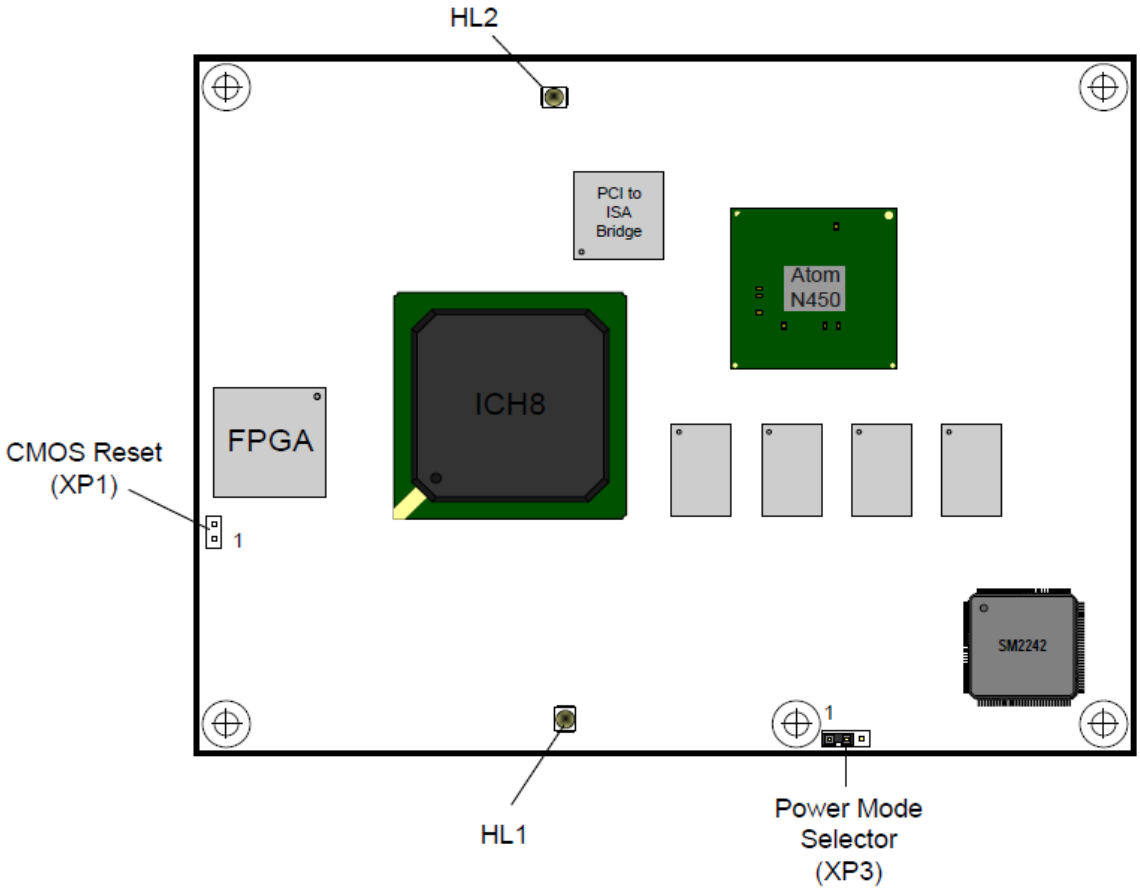
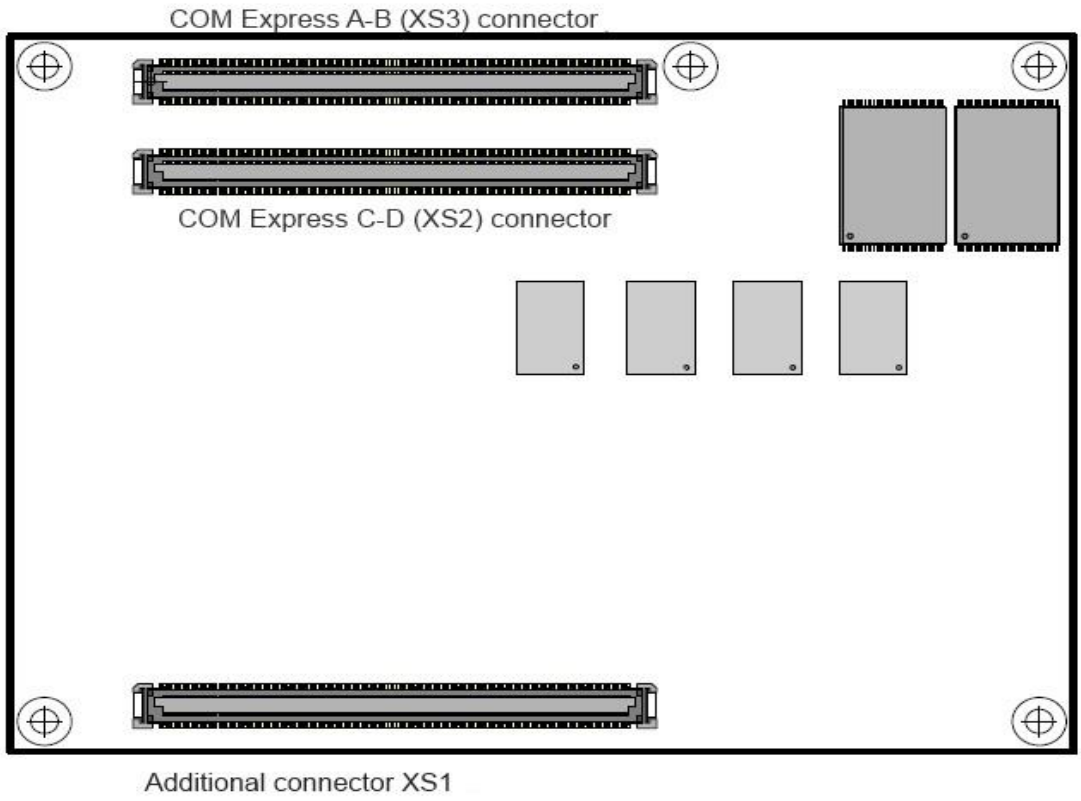


Fig. 3-3: Location of connectors and main components (bottom view)



4. Operation of main components

4.1. Intel PineView-M (-D)

32-bit Intel CPU based on Atom core with low power consumption (~5.5 W). A highly integrated solution, combining the CPU core itself and SDRAM/DDR controller and 2D/3D graphics adapter.

4.2. ICH-8M

A highly integrated interface controller including standard peripherals of the IBM PC AT platform.

4.3. RAM

The board has 1 GB DDR2-667 RAM, soldered, non-extendable.

4.4. BIOS

16 Mb Flash on SPI bus is used for BIOS.

4.5. RTC, CMOS

The real time clock is installed into ICH8. When there is no power, the clock will be operated by a lithium battery installed on the carrier board. The BIOS Setup settings are stored in FRAM.

4.6. FRAM

64 Kb of non-volatile memory can be used for storing user data and BIOS Setup settings.

4.7. NAND Flash

The board is equipped with NAND Flash memory chip with a total volume 4 GB. Location of NAND Flash on SATA bus (SATA Flash Disk Controller is used) enables to increase the operating speed and ensure compatibility with various OS. 2-channel NAND Flash operation mode is ensured.

4.8. Ethernet

Two PCI-E Ethernet 10/100/1000 Mb/s controllers are used on Intel i82574 Ethernet controller. In accordance with PICMG COM.0 r.2.0 specification, one channel is routed to the standard COM Express A-B connector, another one is routed to the additional connector.

4.9. PCI-E

The board has three PCI-E x1 channels. According to PICMG COM.0 r.2.0 specification the signals are routed to the standard COM Express A-B connector.

4.10. IDE

Interface is used for the connection of Compact Flash (Type I/ Type II) and/or ATA storage device; and according to the PICMG COM.0 r.2.0 specification is routed to the standard COM Express C-D connector.

4.11. USB 2.0

The board has eight USB 2.0 channels which according to PICMG COM.0 r.2.0 specification are routed to the standard COM Express A-B connector.

4.12. SATA

2x interfaces (SATA0 и SATA1) for the connection of storage devices are routed to the standard COM Express A-B connector in accordance with PICMG COM.0 r.2.0 specification.

4.13. Audio

Interface for the connection of HD Audio controller is routed to the standard COM Express A-B connector in accordance with PICMG COM.0 r.2.0 specification.

4.14. VGA, LVDS

The ports are designed for the connection of analog VGA monitor and /or LVDS display. Support of two-display configurations, clone/extended desktop. The ports are routed to the standard COM Express A-B connector in accordance with PICMG COM.0 r.2.0 specification.

4.15. Digital I/O

2x programmable digital I/O ports are available. The digital I/O controller is implemented in FPGA as a device on LPC bus. Signals of the first port are routed to the standard COM Express A-B connector in accordance with PICMG COM.0 r.2.0 specification, signals of the second are routed to the additional connector.

4.16. ISA bus [1]

ITE PCI-ISA IT8888 Bridge is used. The signals are routed to the additional connector. Allocation of I/O address space is given in the table below.

[1] - 1) For versions -02, -04 when KIB1283-01 carrier board is used

Table. 4-1: Purpose of I/O address space

Range of addresses	Function	Note
0100h – 016Fh	Access to external ISA bus	
0178h – 01EFh	Access to external ISA bus	
01F8h – 01FFh	Access to external ISA bus	
0210h – 02E7h	Access to external ISA bus	
02F0h – 02F7h	Access to external ISA bus	
0320h – 0375h	Access to external ISA bus	
03E0h – 03E7h	Access to external ISA bus	
0400h – 04CFh	Access to external ISA bus	
04D2h – 04FFh	Access to external ISA bus	
0580h – 0777h	Access to external ISA bus	
0780h – 0CF8h	Access to external ISA bus	
0D00h – 0FFFh	Access to external ISA bus	

Table 4-2: Allocation of interrupt lines

Interrupt	Primary purpose (by default)	Alternative source
IRQ0	System Time Clock	
IRQ1	Keyboard	
IRQ2	Interrupt 8259	
IRQ3	-	COM2, COM4 where KIB1283 is used
IRQ4	-	COM1, COM3 where KIB1283 is used
IRQ5	Internal PCI device on CPC1310	IRQ5 line of external ISA
IRQ6	-	IRQ6 line of external ISA
IRQ7	-	LPT where KIB1283 is used
IRQ8	RTC (Real-time Clock)	-
IRQ9	ACPI	IRQ9 line of external ISA
IRQ10	Internal PCI device on CPC1310	IRQ10 line of external ISA
IRQ11	Internal PCI device on CPC1310	IRQ11 lien of external ISA
IRQ12	Mouse	-
IRQ13	Redundant for mathematical coprocessor	-
IRQ14	Compact Flash	-
IRQ15	-	-

4.17. PCI bus

PCI 32-bit interface with the frequency of 33 MHz. Signals are routed to the standard COM Express C-D connector in accordance with PICMG COM.0 r.2.0 specification.

4.18. LPC bus

The bus is designed for connection of SMSC Super I/O SCH3114 I/O controller or Winbond W83627HF-AW, as well as FPGA. Signals are routed to the standard COM Express A-B connector according to PICMG COM.0 r.2.0 specification.

4.19. I2C bus

I2C controller is implemented in FPGA as a device on LPC bus. The controller supports "Master" mode and operates at the frequency of 600 kHz. Registers are available via 302h/303h I/O ports. For accessing the registers it is required to write two successive values: 46h, and then 57h to the port 302h. While the two successive values: 57h and then 46h are written to the port 302h, access to the registers is blocked. Index is written to port 302h, data is written/read via port 303h.
Registers of I2C controller and their description are given in the tables below:

Table 4-3: Table of I2C bus registers

Address of I/O port	**Configuration register**
Base+0	Address register
Base+1	Control register
Base+2	Status register
Base+3	Data register
Base+4	Timeout register

Table 4-4: Description of address register (Base+0)

#	**Type**	**Register state after reset**	**Description**
7-0	R/W	00h	I2C controller address in Slave mode. The least significant bit always equals to 0.

Table 4-5: Description of control register (Base+1)

Bit number	**Type**	**Register condition after reset**	**Description**
7	R/W	0	Enable bit of I2C controller interrupts. 0 – interrupts are prohibited 1 – interrupts are permitted
6	R/W	0	Enable bit of I2C controller interrupts. 0 – interrupts are prohibited 1 – interrupts are permitted
5	R/W	0	Bit of Master/Slave mode selection. When the bit state is changed: 0 → 1, I2C controller generates the START state and changes to Master

			mode. When the bit state is changed: 1 → 0, I2C controller enters Slave mode and, if the bit held bus, STOP state is generated
4	R/W	0	Exchange direction bit on I2C bus in Master/Slave modes. 0 – Data receipt 1 – Data transfer
3	R/W	0	State installed on I2C bus by receiver using Master and Slave modes for confirmation of byte acceptance. 0 – confirm byte acceptance, 1 – byte acceptance is not confirmed. When byte is accepted in Master mode, Set to 1 means that the cycle of data reception from Slave device is completed.
2	R/W	0	START state repeat bit on I2C bus. 0 – End of START state on I2C bus. 1 – Repeat START state on I2C bus upon completion of byte transfer/receipt.
1-0	R/W	0	Selector of exchange rate on I2C bus. 00 – 94696 baud 01 – 189393 baud 10 – 378787 baud 11 – 757575 baud

Table 4-6: Description of status register (Base+2)

#	**Type**	**Register state after reset**	**Description**
7	R	0	Flag of byte transfer completion on I2C bus. 0 – Completion of ACK state on I2C bus 1 – Change to ACK state on I2C bus

6	R	0	Addressing flag in the Slave mode. If address on I2C bus matches the address in I2C address register, is set to 1.
5	R	0	Bit of I2C bus holding. The bit is set, if the START state is detected on bus. Will be reset when the STOP state on bus is detected. 0 –I2C bus is available 1 –I2C bus is not available
4	R/W	0	Bit of control loss on I2C bus. 1 – Control on I2C bus is lost. It is required to write 0 in order to reset to this bit.
3	R	0	Bit of ACK state completion (confirmation of the received data) on I2C bus. 0 – ACK state hasn't been passed 1 – ACK state has been passed
2	R	0	Bit of transfer direction in Slave mode. 0 – Data receipt 1 – Data transfer

#	Type	Register state after reset	Description
1	R/W	0	Interrupt flag from I2C controller. Will be set to 1 when there is a permitted interrupt (see bit of the 6th I2C control register) and control loss on bus (see bit 4), change to ACK state on bus (see bit 7), ACK state completion on the bus (see bit 3), as well as setting the addressing flag in the Slave mode (see bit 6). In order to reset to this bit it is required to write 0 in the interrupt handler.
0	R	0	State bit on I2C bus, when confirmation bit is received upon completion of each byte transfer. 0 – ACKNOWLEDGE state is accepted 1 – NOT ACKNOWLEDGE state is accepted

Table 4-7: Description of data register (Base+3)

#	Type	Register state after reset	Description
7-0	R/W	-	Data for transfer mode during writing process or receipt mode data during reading.

Table 4-8: Description of timer setting register (Base+4)

#	Type	Register state after reset	Description
7-0	R/W	-	Timeout register of change to the STOP state on I2C bus after completion of byte transfer/receipt. 00h – Transfer immediately after completion of byte transfer/receipt, 01h..0FEh – change after 1..254 cycles of reference frequency (33 MHz) FFh –I2C controller is in the active condition with anticipation of the next byte awaiting the next byte to be written.

4.20. Digital I/O signals

GPIO and DIO registers make it possible to read and set GPI[3:0], GPO[3:0] I/O signals routed to COM Express connector and DIO[7:0] signals, routed to the additional connector.

The registers are available via 302h/303h I/O ports. For accessing the registers it is required to write two successive values: 46h, and then 57h to the port 302h. While the two successive values: 57h and then 46h are written to the port 302h, access to the registers is blocked. Index is written to port 302h, data is written/read via port 303h.

Table 4-9: Description of DIO setting register

Offset index	#	**Type**	**Register state after reset**	**Description**
	7	R/W	1	Control bit of DIO7 channel. 0 – sets the DIO7 line to logic 0 1 – sets the DIO7 into a high-impedance Z-state. In which case the DIO7 line can be used as digital input, and a logical 1 will be set on the line due to a pull-up resistor.
	6	R/W	1	Control bit of DIO6 channel. 0 - sets the DIO6 line to logic 0 1 – sets the DIO6 into a high-impedance Z-state. In which case the DIO6 line can be used as digital input, and a logical 1 will be set on the line due to a pull-up resistor.
	5	R/W	1	Control bit of DIO5 channel. 0 - sets the DIO5 line to logic 0 1 – sets the DIO5 into a high-impedance Z-state. In which case the DIO5 line can be used as digital input, and a logical 1 will be set on the line due to a pull-up resistor.
	4	R/W	1	Control bit of DIO4 channel. 0 - sets the DIO4 line to logic 0 1 – sets the DIO4 into a high-impedance Z-state. In which case the DIO4 line can be used as digital input,

				and a logical 1 will be set on the line due to a pull-up resistor.
	3	R/W	1	Control bit of DIO3 channel. 0 - sets the DIO3 line to logic 0 1 – sets the DIO3 into a high-impedance Z-state. In which case the DIO3 line can be used as digital input, and a logical 1 will be set on the line due to a pull-up resistor.
	2	R/W	1	Control bit of DIO2 channel. 0 - sets the DIO2 line to logic 0 1 – sets the DIO2 into a high-impedance Z-state. In which case the DIO2 line can be used as digital input, and a logical 1 will be set on the line due to a pull-up resistor.
01h	1	R/W	1	Control bit of DIO1 channel. 0 - sets the DIO1 line to logic 0 1 – sets the DIO1 into a high-impedance Z-state. In which case the DIO1 line can be used as digital input, and a logical 1 will be set on the line due to a pull-up resistor.
	0	R/W	1	Control bit of DIO0 channel. 0 - sets the DIO0 line to logic 0 1 – sets the DIO0 into a high-impedance Z-state. In which case the DIO0 line can be used as digital input, and a logical 1 will be set on the line due to a pull-up resistor..

Offset index	#	Type	Register state after reset	Description
02h	7	R	-	State bit of DIO7 line. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line
	6	R	-	State bit of DIO6 line. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line
	5	R	-	State bit of DIO5 line. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line
	4	R	-	State bit of DIO4 line. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line
	3	R	-	State bit of DIO3 line. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line
	2	R	-	State bit of DIO2 line. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line
	1	R	-	State bit of DIO1 line. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line
	0	R	-	State bit of DIO0 line. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line

Table 4-10: Description of GPIO setting register

Offset index	#	Type	Register state after reset	Description
03h	7	R/W	1	Control bit of COMEX_GPIN3 digital I/O channel. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line
	6	R/W	1	Control bit of COMEX_GPIN2 digital I/O channel. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line
	5	R/W	1	Control bit of COMEX_GPIN1 digital I/O channel. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line
	4	R/W	1	Control bit of COMEX_GPIN0 digital I/O channel. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line
	3	R/W	1	Control bit of COMEX_GPOUT3 digital I/O channel. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line
	2	R/W	1	Control bit of COMEX_GPOUT2 digital I/O channel. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line
	1	R/W	1	Control bit of COMEX_GPOUT1 digital I/O channel. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line
	0	R/W	1	Control bit of COMEX_GPOUT0 digital I/O channel. 0 – Logic 0 is set on the line 1 – Logic 1 is set on the line

4.21. SMBus

SMBus (System Management Bus) ensures monitoring and system configuration functions. This bus uses 2-wire interface I2C™. Below is a table with addresses of SMBus devices:

Table 4-11: Addresses of SMBus devices

Address on bus	Description
D2h	Clock unit SLG8SP533
2Eh	LM87 chip
50h	AT24C02C chip
51h	AT24C02C chip

4.22. Watchdog

The board is equipped with two watchdog timers, one (WDT1) is integrated into supervisor chip and has a fixed actuation interval (1,6 s), another one is integrated into FPGA chip and has a programmed actuation interval. Activation of the watchdog timer and hardware interrupt selection (IRQ) is carried out in BIOS Setup. Timer operation is performed via registers in the field of I/O ports. The registers are available via 302h/303h I/O ports. For accessing the registers, two successive values: 46h and then 57h will need to be written to the port 302h. While the two successive values: 57h and then 46h are written to the port 302h, access to the registers is blocked. Index is written to port 302h, data is written/read via port 303h.

The I/O registers of WDT-controller are described in the table below.

Table 4-12: Description of timer setting register

Offset index	**#**	**Type**	**Register state after reset**	**Description**
04h	7-0	R/W	00h	Actuation timeout register of watchdog timer. Timeout can have values ranging from 1 to 255 minutes/s (depending on a bit of the 7th configuration register of watchdog timer, see register 05h below). When 00h value is written, the watchdog timer is switched off. While reading, timeout value is given in minutes/seconds, left until watchdog timer actuation. In order to reset the switched-on watchdog timer, the application software should write a zero value to this register within the selected timeout.
05h	0	R	0	Watchdog timer actuation flag. 1 – Watchdog timer has been actuated 0 – Watchdog timer has not been actuated. For resetting the bit to 0, it is required to write any value to the actuation timeout register of watchdog timer (see register 04h above).
	1	-	-	-
	2	-	-	-
	3	-	-	-
	4	-	-	-
	5	-	-	-
	6	-	-	-
	7	R/W	0	Control bit of the watchdog timeout 0 – Actuation timeout of watchdog timer is measured in minutes 1 - Actuation timeout of watchdog timer is measured in seconds

4.23. LEDs

The board has two LEDs HL1 and HL2. Location of the LEDs is shown on Fig. 3-2. Purpose and description of LED states are given in the following table:

Table 4-13: Purpose of LEDs

Name	Color	State
HL1	Flashing red	Activities on SATA and IDE buses while accessing the storage devices.
HL2	Red	LED is ON when there is voltage +5V_STBY
	Yellow	Standby mode (S4)
	Green	All the board power supplies are operating in the standard mode

4.24. Reset and power monitoring

CPU reset signal is generated from the following sources:

- Supervising device when the power supply is switched on;
- By "RESET" button (from carrier board);
- From watchdog timers.

4.25. Switches (Jumpers)

The board has switches of the following functions:

- CMOS Reset switch;
- Switch of the power supply operation mode: from ATX power supply unit, corresponding to r2.2 specifications (with the use of PS_ON# signal), or from a power supply with an extended voltage range.

Positions of switches, as per their functions, are given in Section 7 Configuration.

5. Interfaces and connectors

5.1. COM Express A-B, C-D connectors

CPC1310 board is equipped with standard COM Express connectors (see Fig. 3-3: Location of connectors and major components (bottom view)), used by CPC1310 to connect with TYPE II carrier board, corresponding to the PICMG COM.0 r.2.0 specification. Purpose of the contacts for each of the connectors is shown in the tables below.

Table 5-1: Purpose of XS3 connector's outputs

A-B Connector (XS3)					
Contact	Description	Note	Contact	Description	Note
A1	GND (FIXED)		B1	GND (FIXED)	
A2	GBE0_MDI3-		B2	GBE0_ACT#	
A3	GBE0_MDI3+		B3	LPC_FRAME	
A4	GBE0_LINK100#		B4	LPC_AD0	
A5	GBE0_LINK1000#		B5	LPC_AD1	
A6	GBE0_MDI2-		B6	LPC_AD2	
A7	GBE0_MDI2+		B7	LPC_AD3	
A8	GBE0_LINK#		B8	LPC_DRQ0#	
A9	GBE0_MDI1-		B9	LPC_DRQ1#	
A10	GBE0_MDI1+		B10	LPC_CLK	
A11	GND (FIXED)		B11	GND (FIXED)	
A12	GBE0_MDI0-		B12	PWRBTN#	Pull-up 10K to 3.3V STBY
A13	GBE0_MDI0+		B13	SMB_CK	Pull-up 2.2K to 3.3V STBY
A14	GBE0_CTREF		B14	SMB_DAT	Pull-up 2.2K to 3.3V STBY
A15	SUS_S3#		B15	SMB_ALERT#	Pull-up 10K to 3.3V STBY
A16	SATA0_TX+		B16	SATA1_TX+	
A17	SATA0_TX-		B17	SATA1_TX-	
A18	SUS_S4#		B18	SUS_STAT#	Pull-up 10K to 3.3V STBY
A19	SATA0_RX+		B19	SATA1_RX+	
A20	SATA0_RX-		B20	SATA1_RX-	
A21	GND (FIXED)		B21	GND (FIXED)	
A22	SATA2_TX+	Not used	B22	SATA3_TX+	Not used
A23	SATA2_TX	Not used	B23	SATA3_TX-	Not used
A24	SUS_S5#		B24	PWR_OK	Pull-up 100K to 3.3V STBY
A25	SATA2_RX+	Not used	B25	SATA3_RX+	Not used
A26	SATA2_RX-	Not used	B26	SATA3_RX-	Not used
A27	BATLOW#	Pull-up 10K to 3.3V STBY	B27	WDT	
A28	ATA_ACT#	Pull-up 10K to 3.3V	B28	AC_SDIN2	
A29	AC_SYNC		B29	AC_SDIN1	
A30	AC_RST#		B30	AC_SDIN0	
A31	GND (FIXED)		B31	GND (FIXED)	

A-B Connector (XS3)					
Contact	Description	Note	Contact	Description	Note
A32	AC_BITCLK		B32	SPKR	
A33	AC_SDOUT		B33	I2C_CK	Pull-up 2.2K to 3.3V
A34	BIOS_DISABLE#	Pull-up 10K to 3.3V STBY	B34	I2C_DAT	Pull-up 2.2K to 3.3V
A35	THRMTRIP#		B35	THRM#	Pull-up 10K to 3.3V
A36	USB6-		B36	USB7-	
A37	USB6+		B37	USB7+	
A38	USB_6_7_OC#	Pull-up 10K to 3.3V STBY	B38	USB_4_5_OC#	Pull-up 10K to 3.3V STBY
A39	USB4-		B39	USB5-	
A40	USB4+		B40	USB5+	
A41	GND (FIXED)		B41	GND (FIXED)	
A42	USB2-		B42	USB3-	
A43	USB2+		B43	USB3+	
A44	USB_2_3_OC#	Pull-up 10K to 3.3V STBY	B44	USB_0_1_OC#	Pull-up 10K to 3.3V STBY
A45	USB0-		B45	USB1-	
A46	USB0+		B46	USB1+	
A47	VCC_RTC		B47	EXCD1_PERST#	
A48	EXCD0_PERST#		B48	EXCD1_CPPE#	Pull-up 10K to 3.3V
A49	EXCD0_CPPE#	Pull-up 10K to 3.3V	B49	SYS_RESET#	Pull-up 10K to 3.3V
A50	LPC_SERIRQ	Pull-up 10K to 3.3V	B50	CB_RESET#	Pull-down 10K to GND
A51	GND (FIXED)		B51	GND (FIXED)	
A52	PCIE_TX5+	Not Used	B52	PCIE_RX5+	Not used
A53	PCIE_TX5-	Not Used	B53	PCIE_RX5-	Not used
A54	GPI0	Pull-up 5k÷16.5k to 3.3V	B54	GPO1	
A55	PCIE_TX4+	Not Used	B55	PCIE_RX4+	
A56	PCIE_TX4-	Not Used	B56	PCIE_RX4-	
A57	GND		B57	GPO2	
A58	PCIE_TX3+		B58	PCIE_RX3+	
A59	PCIE_TX3-		B59	PCIE_RX3-	
A60	GND (FIXED)		B60	GND_(FIXED)	
A61	PCIE_TX2+		B61	PCIE_RX2+	
A62	PCIE_TX2-		B62	PCIE_RX2-	
A63	GPI1	Pull-up 5k÷16.5k to 3.3V	B63	GPO3	
A64	PCIE_TX1+		B64	PCIE_RX1_+	
A65	PCIE_TX1-		B65	PCIE_RX1-	
A66	GND		B66	WAKE0#	Pull-up 1K to 3.3V STBY
A67	GPI2	Pull-up 5k÷16.5k to 3.3V	B67	WAKE1#	Pull-up 10K to 3.3V
A68	PCIE_TX0+		B68	PCIE_RX0+	
A69	PCIE_TX0-		B69	PCIE_RX0-	
A70	GND (FIXED)		B70	GND (FIXED)	
A71	LVDS_A0+		B71	LVDS_B0+	Not used
A72	LVDS_A0-		B72	LVDS_B0-	Not used
A73	LVDS_A1+		B73	LVDS_B1+	Not used

A-B Connector (XS3)					
Contact	Description	Note	Contact	Description	Note
A74	LVDS_A1-		B74	LVDS_B1-	Not used
A75	LVDS_A2+		B75	LVDS_B2+	Not used
A76	LVDS_A2-		B76	LVDS_B2-	Not used
A77	VDS_VDD_EN		B77	LVDS_B3+	Not used
A78	LVDS_A3+	Not used	B78	LVDS_B3-	Not used
A79	LVDS_A3-	Not used	B79	LVDS_BKLT_EN	
A80	GND (FIXED)		B80	GND (FIXED)	
A81	LVDS_A_CK+		B81	LVDS_B_CK+	Not used
A82	LVDS_A_CK-		B82	LVDS_B_CK-	Not used
A83	LVDS_I2C_CK	Pull-up 2.2K to 3.3V	B83	LVDS_BKLT_CTRL	
A84	LVDS_I2C_DAT	Pull-up 2.2K to 3.3V	B84	VCC_5V_SBY	
A85	GPI3	Pull-up 5k÷16.5k to 3.3V	B85	VCC_5V_SBY	
A86	KBD_RST#	Pull-up 5K to 3.3V	B86	VCC_5V_SBY	
A87	KBD_A20GATE	Pull-up 5K to 3.3V	B87	VCC_5V_SBY	
A88	PCIE0_CK_REF+		B88	BIOS_DIS1#	Pull-up 10K to 3.3V STBY
A89	PCIE0_CK_REF-		B89	VGA_RED	
A90	GND (FIXED)		B90	GND (FIXED)	
A91	SPI_POWER		B91	VGA_GRN	
A92	SPI_MISO		B92	VGA_BLU	
A93	GPO0		B93	VGA_HSYNC	
A94	SPI_CLK		B94	VGA_VSYNC	
A95	SPI_MOSI		B95	VGA_I2C_CK	Pull-up 2.2K to 3.3V
A96	GND		B96	VGA_I2C_DAT	Pull-up 2.2K to 3.3V
A97	TYPE10#	Not used	B97	SPI_CS#	
A98	RSVD		B98	RSVD	
A99	RSVD		B99	RSVD	
A100	GND (FIXED)		B100	GND (FIXED)	
A101	RSVD		B101	RSVD	
A102	RSVD		B102	RSVD	
A103	RSVD		B103	RSVD	
A104	VCC_12V		B104	VCC_12V	
A105	VCC_12V		B105	VCC_12V	
A106	VCC_12V		B106	VCC_12V	
A107	VCC_12V		B107	VCC_12V	
A108	VCC_12V		B108	VCC_12V	
A109	VCC_12V		B109	VCC_12V	
A110	GND (FIXED)		B110	GND (FIXED)	

Note

If a power mode with an extended input range is used, outputs A104 - A109, B84-B87, B104 - B109 are fed with +4,75 ÷ 14 V.

Table 5-2: Purpose of XS2 connector's outputs

C-D Connector (XS2)					
Contact	Description	Note	Contact	Description	Note
C1	GND (FIXED)		D1	GND (FIXED)	
C2	IDE_D7		D2	IDE_D5	
C3	IDE_D6		D3	IDE_D10	
C4	IDE_D3		D4	IDE_D11	
C5	IDE_D15		D5	IDE_D12	
C6	IDE_D8		D6	DE_D4	
C7	IDE_D9		D7	IDE_D0	
C8	IDE_D2		D8	IDE_REQ	
C9	IDE_D13		D9	IDE_IOW#	
C10	IDE_D1		D10	IDE_ACK#	
C11	GND (FIXED)		D11	GND (FIXED)	
C12	IDE_D14		D12	IDE_IRQ	Pull-up 10K to 3.3V
C13	IDE_IORDY	Pull-up 10K to 3.3V	D13	IDE_A0	
C14	IDE_IOR#		D14	IDE_A1	
C15	PCI_PME#	Pull-up 10K to 3.3V_STBY	D15	IDE_A2	
C16	PCI_GNT2#		D16	IDE_CS1#	
C17	PCI_REQ2#	Pull-up 10K to 3.3V	D17	IDE_CS3#	
C18	PCI_GNT1#		D18	IDE_RESET#	Pull-down 100K
C19	PCI_REQ1#	Pull-up 10K to 3.3V	D19	PCI_GNT3#	Not used on CPC1310-01,-03
C20	PCI_GNT0#	Pull-up 10K to 3.3V_STBY	D20	PCI_REQ3#	Pull-up 10K to 3.3V, Not used on CPC1310-01,-03
C21	GND (FIXED)		D21	GND (FIXED)	
C22	PCI_REQ0#	Pull-up 10K to 3.3V	D22	PCI_AD1	
C23	PCI_RESET#	Pull-down 100K to GND	D23	PCI_AD3	
C24	PCI_AD0		D24	PCI_AD5	
C25	PCI_AD2		D25	PCI_AD7	
C26	PCI_AD4		D26	PCI_C/BE0#	
C27	PCI_AD6		D27	PCI_AD9	
C28	PCI_AD8		D28	PCI_AD11	
C29	PCI_AD10		D29	PCI_AD13	
C30	PCI_AD12		D30	PCI_AD15	
C31	GND (FIXED)		D31	GND (FIXED)	
C32	PCI_AD14		D32	PCI_PAR	
C33	PCI_C/BE1#		D33	PCI_SERR#	Pull-up 10K to 3.3V
C34	PCI_PERR#	Pull-up 10K to 3.3V	D34	PCI_STOP#	Pull-up 10K to 3.3V
C35	PCI_LOCK#	Pull-up 10K to 3.3V	D35	PCI_TRDY#	Pull-up 10K to 3.3V
C36	PCI_DEVSEL#	Pull-up 10K to 3.3V	D36	PCI_FRAME#	Pull-up 10K to 3.3V
C37	PCI__IRDY#	Pull-up 10K to 3.3V	D37	PCI_AD16	
C38	PCI_C/BE2#		D38	PCI_AD18	
C39	PCI_AD17		D39	PCI_AD20	
C40	PCI_AD19		D40	PCI_AD22	
C41	GND (FIXED)		D41	GND (FIXED)	

C-D Connector (XS2)					
Contact	Description	Note	Contact	Description	Note
C87	GND		D87	GND	
C88	PEG_RX11+		D88	PEG_TX11+	Not used
C89	PEG_RX11-		D89	PEG_TX11-	Not used
C90	GND_(FIXED)		D90	GND_(FIXED)	
C91	PEG_RX12+		D91	PEG_TX12+	Not used
C92	PEG_RX12-		D92	PEG_TX12-	Not used
C93	GND		D93	GND	
C94	PEG_RX13+		D94	PEG_TX13+	Not used
C95	PEG_RX13-		D95	PEG_TX13-	Not used
C96	GND		D96	GND	
C97	RSVD		D97	PEG_ENABLE#	Not used
C98	PEG_RX14+		D98	PEG_TX14+	Not used
C99	PEG_RX14-		D99	PEG_TX14-	Not used
C100	GND (FIXED)		D100	GND (FIXED)	
C101	PEG_RX15+		D101	PEG_TX15+	Not used
C102	PEG_RX15-		D102	PEG_TX15-	Not used
C103	GND		D103	GND	
C104	VCC_12V		D104	VCC_12V	
C105	VCC_12V		D105	VCC_12V	
C106	VCC_12V		D106	VCC_12V	
C107	VCC_12V		D107	VCC_12V	
C108	VCC_12V		D108	VCC_12V	
C109	VCC_12V		D109	VCC_12V	
C110	GND (FIXED)		D110	GND (FIXED)	

Note

If a power mode with an extended input range is used, outputs C104 - C109, D104 - D109 are fed with +4,75 ÷ +14 V.

5.2. XS1 additional connector

This connector is installed in versions CPC1310-02 and CPC1310-04.

Table 5-3: Purpose of XS1 connector's outputs

A-B Additional Connector (XS1)					
Contact	Description	Note	Contact	Description	Note
A1	GND_(FIXED)		B1	GND_(FIXED)	
A2	Not used		B2	GBE1_MDI3-	
A3	Not used		B3	GBE1_MDI3+	
A4	Not used		B4	GBE1_LINK100#	
A5	Not used		B5	GBE1_LINK1000#	
A6	Not used		B6	GBE1_MDI2-	

A-B Additional Connector (XS1)					
Contact	Description	Note	Contact	Description	Note
A7	Not used		B7	GBE1_MDI2+	
A8	Not used		B8	GBE1_LINK#	
A9	Not used		B9	GBE1_MDI1-	
A10	Not used		B10	GBE1_MDI1+	
A11	GND_(FIXED)		B11	GND_(FIXED)	
A12	Not used		B12	GBE1_MDI0-	
A13	Not used		B13	GBE1_MDI0+	
A14	Not used		B14	GBE1_CTREF	
A15	Not used		B15	GBE1_ACT#	
A16	Not used		B16	Not used	
A17	Not used		B17	Not used	
A18	Not used		B18	Not used	
A19	Not used		B19	Not used	
A20	Not used		B20	Not used	
A21	GND_(FIXED)		B21	GND_(FIXED)	
A22	Not used		B22	Not used	
A23	Not used		B23	Not used	
A24	Not used		B24	Not used	
A25	Not used		B25	Not used	
A26	Not used		B26	Not used	
A27	Not used		B27	Not used	
A28	Not used		B28	Not used	
A29	Not used		B29	Not used	
A30	Not used		B30	Not used	
A31	GND_(FIXED)		B31	GND_(FIXED)	
A32	Not used		B32	Not used	
A33	Not used		B33	Not used	
A34	Not used		B34	Not used	
A35	Not used		B35	Not used	
A36	Not used		B36	Not used	
A37	Not used		B37	Not used	
A38	Not used		B38	Not used	
A39	Not used		B39	Not used	
A40	Not used		B40	Not used	
A41	GND_(FIXED)		B41	GND_(FIXED)	
A42	Not used		B42	FPGA_DIO0	
A43	Not used		B43	FPGA_DIO1	
A44	Not used		B44	FPGA_DIO2	
A45	Not used		B45	FPGA_DIO3	
A46	Not used		B46	FPGA_DIO4	
A47	Not used		B47	FPGA_DIO5	
A48	Not used		B48	FPGA_DIO6	
A49	Not used		B49	FPGA_DIO7	
A50	Not used		B50	Not used	
A51	GND_(FIXED)		B51	GND_(FIXED)	

A-B Additional Connector (XS1)					
Contact	Description	Note	Contact	Description	Note
A52	Not used		B52	Not used	
A53	Not used		B53	Not used	
A54	Not used		B54	Not used	
A55	Not used		B55	Not used	
A56	Not used		B56	ISA_I/O_CHCK#	Pull-up 4.7K to 5.0V
A57	Not used		B57	ISA_SD7	Pull-up 10K to 5.0V
A58	Not used		B58	ISA_SD6	Pull-up 10K to 5.0V
A59	Not used		B59	ISA_SD5	Pull-up 10K to 5.0V
A60	GND_(FIXED)		B60	GND_(FIXED)	
A61	Not used		B61	ISA_SD4	Pull-up 10K to 5.0V
A62	Not used		B62	ISA_SD3	Pull-up 10K to 5.0V
A63	Not used		B63	ISA_SD2	Pull-up 10K to 5.0V
A64	Not used		B64	ISA_SD1	Pull-up 10K to 5.0V
A65	Not used		B65	ISA_SD0	Pull-up 10K to 5.0V
A66	Not used		B66	ISA_I/O_CHRDY	Pull-up 1K to 5.0V
A67	ISA_RESET_DRV		B67	ISA_AEN	Pull-down 10K to GND
A68	ISA_IRQ9	Pull-up 10K to 5.0V	B68	ISA_SA19	Pull-up 10K to 5.0V
A69	ISA_DRQ2	Pull-down 10K to GND	B69	ISA_SA18	Pull-up 10K to 5.0V
A70	GND_(FIXED)		B70	GND_(FIXED)	
A71	ISA_0WS#	Pull-up 4.7K to 5.0V	B71	ISA_SA17	Pull-up 10K to 5.0V
A72	ISA_SMEMW#	Pull-up 1K to 5.0V	B72	ISA_SA16	Pull-up 10K to 5.0V
A73	ISA_SMEMR#	Pull-up 1K to 5.0V	B73	ISA_SA15	Pull-up 10K to 5.0V
A74	ISA_IOW#	Pull-up 8.2K to 5.0V	B74	ISA_SA14	Pull-up 10K to 5.0V
A75	ISA_IOR#	Pull-up 8.2K to 5.0V	B75	ISA_SA13	Pull-up 10K to 5.0V
A76	ISA_DACK3#		B76	ISA_SA12	Pull-up 10K to 5.0V
A77	ISA_DRQ3	Pull-down 10K to GND	B77	ISA_SA11	Pull-up 10K to 5.0V
A78	ISA_DACK1#		B78	ISA_SA10	Pull-up 10K to 5.0V
A79	ISA_DRQ1	Pull-down 10K to GND	B79	ISA_SA9	Pull-up 10K to 5.0V
A80	GND_(FIXED)		B80	GND_(FIXED)	
A81	ISA_REFRESH#		B81	ISA_SA8	Pull-up 10K to 5.0V
A82	ISA_CLK		B82	ISA_SA7	Pull-up 10K to 5.0V
A83	ISA_IRQ7	Pull-up 10K to 5.0V	B83	ISA_SA6	Pull-up 10K to 5.0V
A84	ISA_IRQ6	Pull-up 10K to 5.0V	B84	ISA_SA5	Pull-up 10K to 5.0V

A-B Additional Connector (XS1)					
Contact	Description	Note	Contact	Description	Note
A85	ISA_IRQ5	Pull-up 10K to 5.0V	B85	ISA_SA4	Pull-up 10K to 5.0V
A86	ISA_IRQ4	Pull-up 10K to 5.0V	B86	ISA_SA3	Pull-up 10K to 5.0V
A87	ISA_IRQ3	Pull-up 10K to 5.0V	B87	ISA_SA2	Pull-up 10K to 5.0V
A88	ISA_DACK2#		B88	ISA_SA1	Pull-up 10K to 5.0V
A89	ISA_TC	Pull-down 10K to GND	B89	ISA_SA0	Pull-up 10K to 5.0V
A90	GND_(FIXED)		B90	GND_(FIXED)	
A91	ISA_BALE	Pull-down 10K to GND	B91	ISA_SBHE	
A92	ISA_OSC		B92	ISA_LA23	Pull-up 10K to 5.0V
A93	ISA_MEM_CS16#	Pull-up 4.7K to 5.0V	B93	ISA_LA22	Pull-up 10K to 5.0V
A94	ISA_IO_CS16#	Pull-up 4.7K to 5.0V	B94	ISA_LA21	Pull-up 10K to 5.0V
A95	ISA_IRQ10	Pull-up 10K to 5.0V	B95	ISA_LA20	Pull-up 10K to 5.0V
A96	ISA_IRQ11	Pull-up 10K to 5.0V	B96	ISA_LA19	
A97	ISA_IRQ12	Pull-up 10K to 5.0V	B97	ISA_LA18	
A98	ISA_IRQ15	Pull-up 10K to 5.0V	B98	ISA_LA17	
A99	ISA_IRQ14	Pull-up 10K to 5.0V	B99	ISA_MEMR#	Not used
A100	GND_(FIXED)		B100	GND_(FIXED)	
A101	ISA_DACK0#		B101	ISA_MEMW#	Not used
A102	ISA_DRQ0	Pull-down 10K to GND	B102	ISA_SD8	Pull-up 10K to 5.0V
A103	ISA_DACK5#		B103	ISA_SD9	Pull-up 10K to 5.0V
A104	ISA_DRQ5	Pull-down 10K to GND	B104	ISA_SD10	Pull-up 10K to 5.0V
A105	ISA_DACK6#		B105	ISA_SD11	Pull-up 10K to 5.0V
A106	ISA_DRQ6	Pull-down 10K to GND	B106	ISA_SD12	Pull-up 10K to 5.0V
A107	ISA_DACK7#		B107	ISA_SD13	Pull-up 10K to 5.0V
A108	ISA_DRQ7	Pull-down 10K to GND	B108	ISA_SD14	Pull-up 10K to 5.0V
A109	ISA_MASTER#	Pull-up 8.2K to 5.0V	B109	ISA_SD15	Pull-up 10K to 5.0V
A110	GND_(FIXED)		B110	GND_(FIXED)	

6. Installation

CPC1310 is installed into Fastwel KIB1283 or KIB1280 carrier boards (with limited functionalities).

Note: When KIB1283 or KIB1280 are installed, the board is fed from ATX power supply, corresponding to the r.2.2. specification.

6.1. Safety requirements

In order to properly install CPC1310 it is necessary to strictly follow the bellow safety rules and requirements to prevent device damages and personal injuries. Fastwel Group will not be responsible for any damages as a result of failure to comply with these requirements.

Careful! Be careful when operating the board since heat spreader (and heat-sink, if installed) may be too hot. In addition, the board should not be put on any surfaces or into any packaging until both the board and heat-sink will be cooled down to ambient temperature.

Attention!

Turn off the power supply before installing the module into the carrier-board. Failure to comply with this regulation may damage your health, as well as lead to malfunctions of the board or the whole system.

Warning, ESD Sensitive Device!

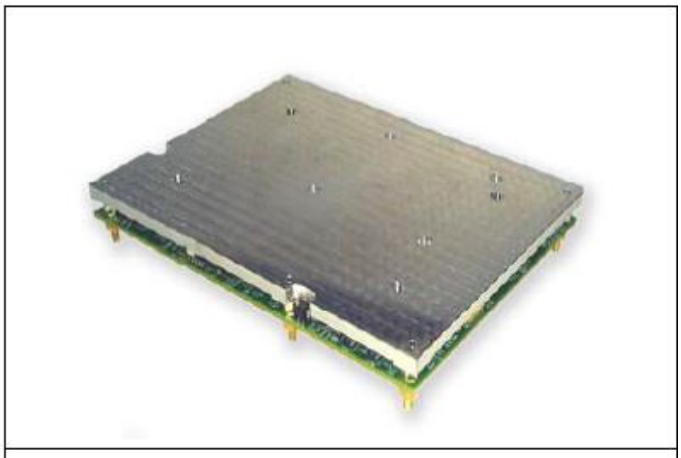
This symbol draws your attention to the information related to electro static sensitivity of your product and its components. To keep product safety and operability it is necessary to handle it with care and comply with the following ESD safety directions:

- Before touching the module, you should discharge the static electricity from your clothes, as well as from tools before their use.
- Do not touch the electronic components and connector contacts.
- If your workplace is equipped with antistatic protection, do not forget to use it. Close attention should be paid in cold and dry weather.

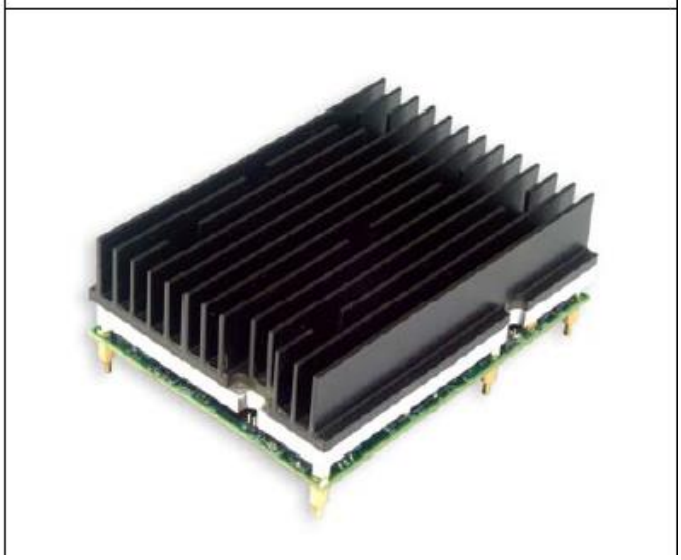
6.2 Possible options for heat removal

Annex A contains information on technical requirements which should be considered by users when developing proprietary cooling system. Temperature should be controlled by using a temperature sensor. Heat removal options are shown on the figure bellow.

Fig. 6-1: Heat removal options



A heat-spreader installed in the upper part of CPC1310. Such a configuration ensures heat dissipation by installing the block directly into the enclosure or chassis (the enclosure serves as a large heat-sink).
Heat is removed from CPU and ICH8 microchip by means of the heat-spreader and is transferred to the enclosure.



Additionally, CPC1310 can be equipped with a finned heat-sink from the ACS30066 kit (to be purchased as an option) or user-manufactured heat-sink. The heat-sink is installed into the heat-spreader (on thermal grease) and fixed by the screws contained in the heat-sink delivery checklist.

6.3. Installation of CPC1310 into the carrier board

In order to install CPC1310 into the carrier-board, follow the bellow procedure:

1. Make sure that safety requirements listed in paragraph 6.1. are met.

Attention!
Noncompliance with the following instructions can cause module damages and system malfunction.

2. Before installation, you'll have to make sure that the module has configuration which corresponds to application requirements. Information on CPC1310 configuration is given in Section 7 Configuration of this User Manual. If user-made heat-sink of the ACS30066 kit is used, and then first you'll have to install the heat-sink, see subsection 6.2.

3. XS3, XS2 and XS1 connectors (versions -02, -04) of CPC1310 (see Fig. 3-3: Location of connectors and main components (bottom view)) should be installed into relevant connectors of the carrier board. Fix the module on the carrier-board with fastening nuts contained in the mounting kit (supplied to the customer with the module), see subparagraph 1.3 of delivery checklist. Nut fastening torque should not exceed 0,1±0,05 N*m in order to prevent thread cutoff on racks.

Attention!

Please note that the heat-spreading plate is electrically connected with signal earth of CPC1310, therefore, if you need to ensure a galvanic isolation between the module and enclosure of the chassis, it is necessary to use a nonconductive material.

6.4. Module removal procedure

To remove the module, please perform the following operations:

1. Make sure that the safety requirements of paragraph 6.1. are met. In particular, pay attention to the warning related to heat-sink temperature!

2. Before start, please make sure that system power supply is switched off.

3. Unscrew fastening nuts and remove the module from carrier-board connectors. Do not touch the heat-sink, since it can become very hot during in operation.

4. Do not put the module into a packaging, until its temperature and temperature of its cooling heat-sinks will be down to ambient temperature.

7. Configuration

7.1 Installation of switches

User has a possibility to configure CPC1310 module with XP1 and XP3 switches (see Fig. 3-3: Location of connectors and main components (bottom view)). General description is given in the table below. Removal/installation of jumpers while the power is ON, **is not allowed**.

Table 7-1: CPC1310 configuration with XP1 and XP3 switches.

Connector's name	Purpose	
XP1	1 and 2 contacts are closed	CMOS Reset (recovery of factory settings)
XP3	1 and 2 are closed (by default)	Fed from ATX power source corresponding to r.2.2 specification (using PS_ON# signal)
	1 and 3 are closed	Extended power supply range from +4,75 V to +14V. The board does not use +5V_STBY voltage with COM Express connector.

7.2. BIOS update

Fwflash.exe utility is designed for updating of BIOS software in module. For updating BIOS you'll need to boot FreeDOS or MSDOS and start fwflash.exe with parameters e.g.:
fwflash.exe /f 1310xxx.bin
1310xxx.bin – file name of the current BIOS version.
For fwflash.exe software utility please visit Fastwel website at: www.fastwel.com


Attention!
FWFLASH.EXE UTILITY OPERATES ONLY UNDER MSDOS, FREEDOS OPERATING SYSTEMS!.


Attention!
RESTART FWFLASH.EXE IF MODIFICATION ERROR MESSAGES ARE DISPLAYED ON THE SCREEN (WITHOUT SWITCHING OFF THE MODULE POWER SUPPLY!).


DO NOT
RECORD BIOS FILES, EXCEPT FOR THOSE SPECIFIED FOR USE BY THE MANUFACTURER AND INCLUDED IN THE MODULE DELIVERY CHECKLIST OR AVAILABLE ON NETWORK FILE-SERVERS OF MANUFACTURER OR OFFICIAL DISTRIBUTOR!

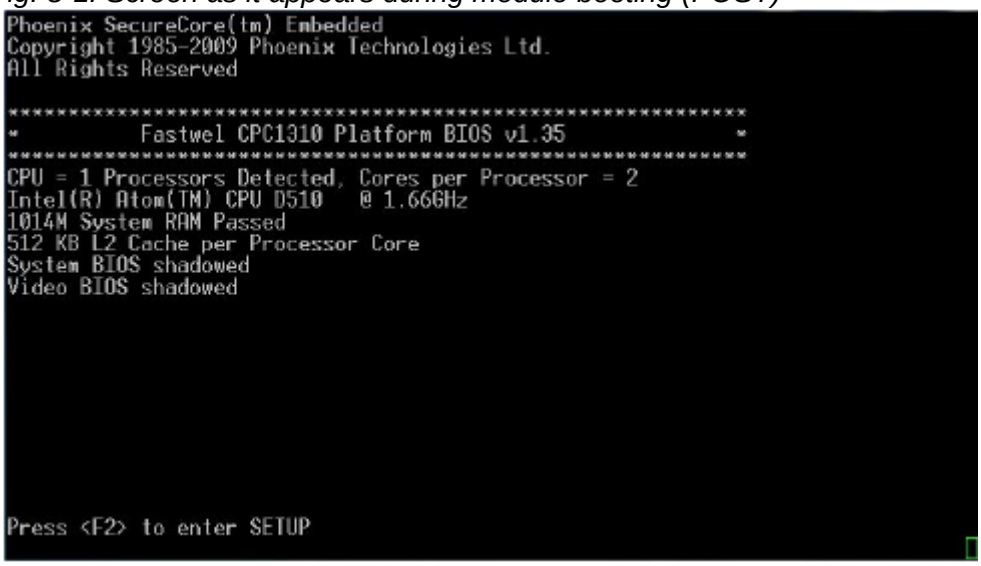
8. Phoenix® BIOS

Your PC has an adapted version of Phoenix® BIOS which is a standard system for IBM PC AT-compatible PCs. It supports Intel®x86 and compatible CPUs, ensures a low-level support for CPU, memory and I/O subsystems. Using BIOS Setup program you can change BIOS parameters and control special modes of PC operation. It helps you changing the basic system settings parameters. These parameters are stored in the FRAM non-volatile memory.

8.1. BIOS Setup start

For starting BIOS Setup program you'll need to press F2 button on the module keyboard or on the keyboard of a console PC (when used as the Hyperterminal's program) at the time of system boot during POST procedure (Power On Self Test). Example of the screen during POST procedure is shown on the figure below.

Fig. 8-1: Screen as it appears during module booting (POST)

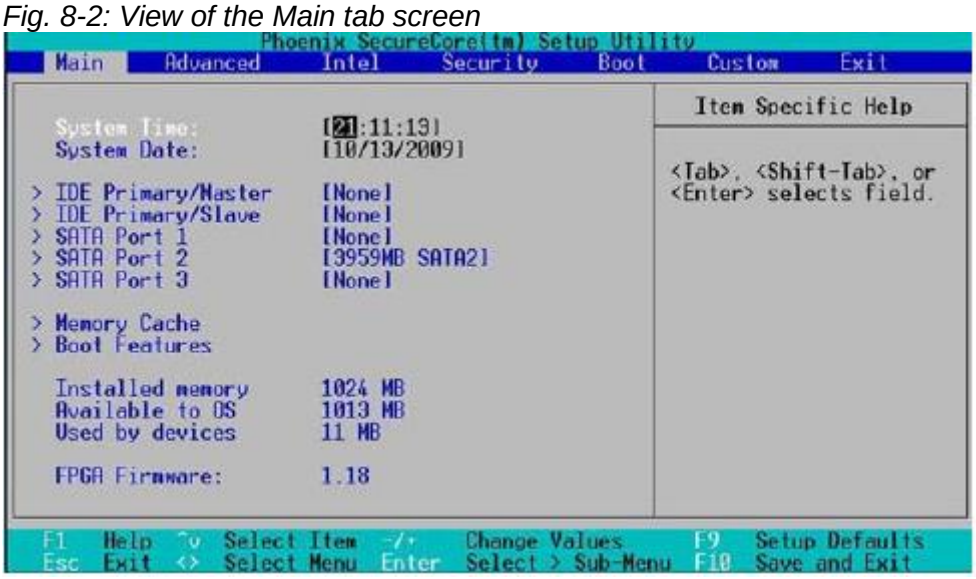


After pressing F2, BIOS Setup menu with an active Main tab will appear.

8.2. Main

This tab of the BIOS Setup program is a heading tab during start. The tab's menu enables to set system clock and date, set parameters of ATA/SATA devices, control caching, set the module booting parameters as well as displays information related to the installed RAM and available for operating systems.

Fig. 8-2: View of the Main tab screen



Note

This description and windows are valid only for SMSC microchip SCH3114. If Winbond SIO microchip is used or if there is no SIO microchip, contents of the windows will be changed.

In order to move through menu options, use Up and Down cursor control keys. In order to move through tabs: use Left and Right cursor control keys. For entering to the settings submenu, use Enter, and Escape – for exiting the settings submenu. In order to change any values in a menu option selected, use + and – keys on the numeric keyboard.

Note

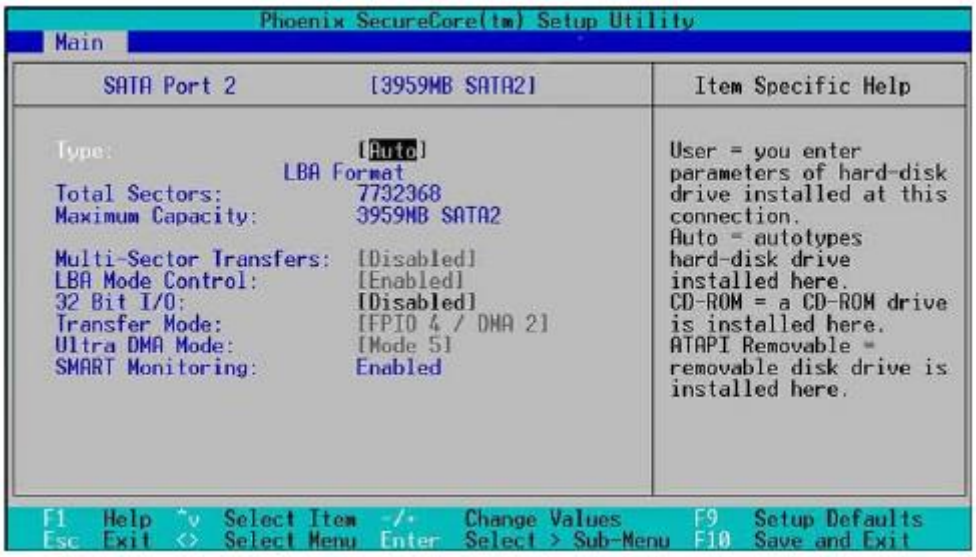
This operating algorithm with menu applies to all other BIOS Setup tabs.

While selecting menu options of ATA/SATA-devices, cashing options, module startup parameters, new submenu screens become available.

The Figure below shows the screen of SATA Port 2 submenu.

8.3. SATA Port 2

Fig. 8-3: Screen of SATA Port 2 submenu

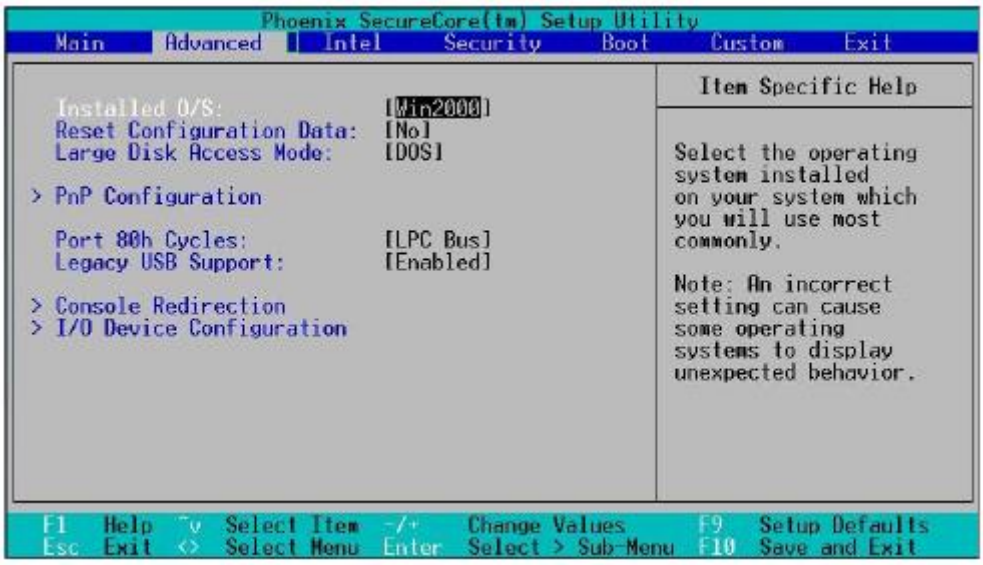


Where:
Type: selection of the storage device:
[Auto] – system automatically selects a type of the storage device
[None] – ATA-storage device is off
[ATAPI Removable], [IDE Removable] – removable ATAPI, IDE devices
[CD-ROM] – CD-ROM drive
[Other ATAPI] – Other devices
[User] – ATA-device parameters are specified by the user
Multi-Sector Transfers: Control of multi-sector data transfer
LBA Mode Control:
32 Bit I/O: Control of 32-bit I/O
Transfer Mode: Selection of a data transfer mode (PIO, DMA)
Ultra DMA Mode: Selection of Ultra DMA mode
SMART Monitoring: S.M.A.R.T. mode monitoring

8.4. Advanced

This tab is used for additional module settings. The Figure below shows the Advanced tab menu.

Fig. 8-4: Screen of Advanced tab



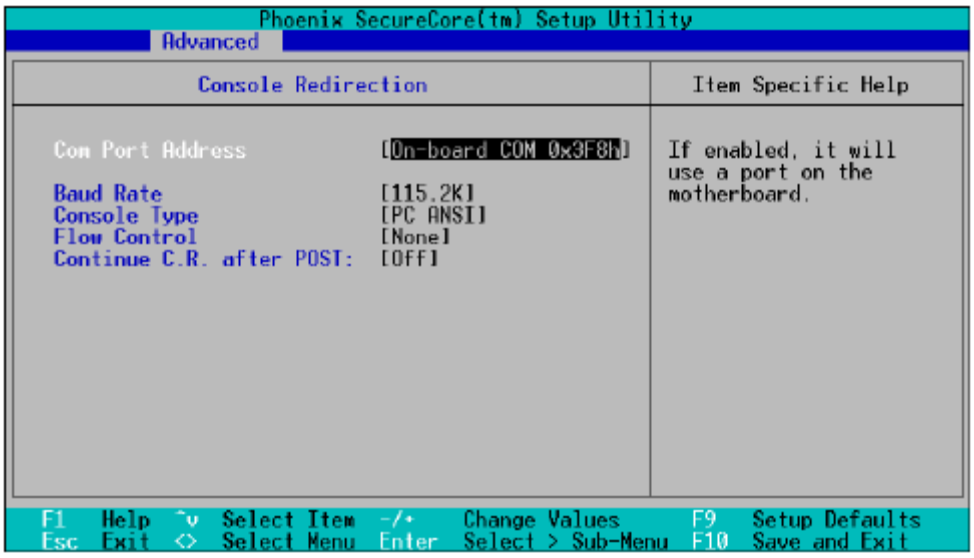
Where:
Installed O/S: Selection of the operating system type installed in the module
Reset Configuration Data: Control of the cleaning of Extended System Configuration Data (ESCD) area.
Large Disk Access Mode: Selection of the Large Disk Access mode
Port 80h Cycles: Selection of a bus for transferring the debugging data via 80h port
Legacy USB Support: Control of USB-devices support at the BIOS level

PnP Configuration submenu is described in subparagraph 8.3.2.

8.4.1. Console Redirection

Submenu of the console redirection settings (port address, speed, type, flow control). Submenu type is shown on the figure below.

Fig. 8-5: Screen of Console Redirection submenu



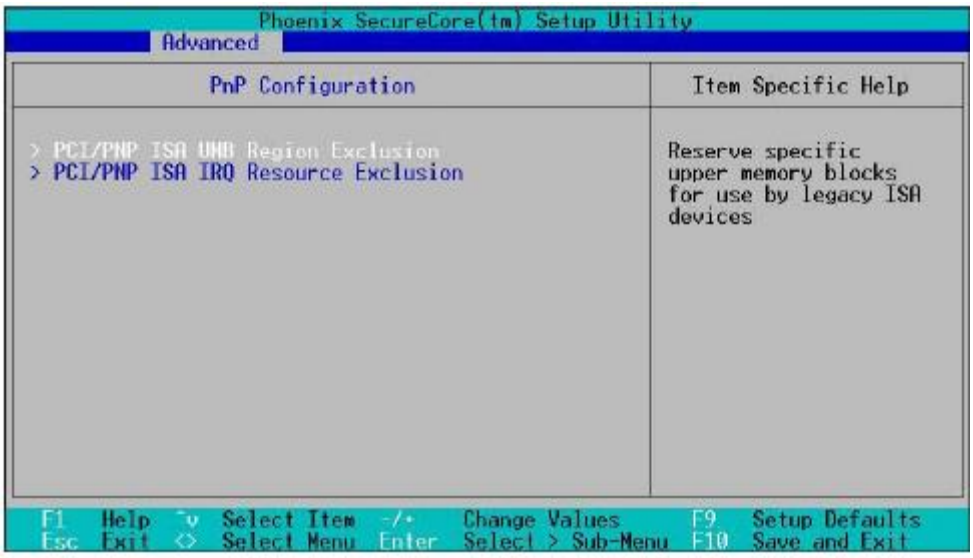
Where:
Com Port Address: - Selection of COM-port for console redirection
[On-board COM 0x3F8h] – COM1
[On-board COM 0x2F8h] – COM2
[Disabled] – Console redirection is disabled

Baud Rate – data transmission rate during operation with the console (300 – 115.2K)
Console Type
Flow Control – Flow control settings
Continue C.R. after POST: - Control of the console redirection process after booting of operating system.

8.4.2 PnP Configuration

Submenu of interrupt distribution settings and memory between PCI- and ISA-devices. Submenu type is shown on the figure below.

Fig. 8-6: Screen of PnP Configuration submenu



Where:

PCI/PNP ISA UMB Region Exclusion

Submenu of the specific upper memory block reservation for the use of ISA bus devices. While opening this submenu, several address ranges in storage space will be displayed, and values [Available] or [Reserved] can be set for each separate range, where:

[Available] – is a memory area available for PCI-devices
[Reserved] – is a memory area reserved for ISA-bus.

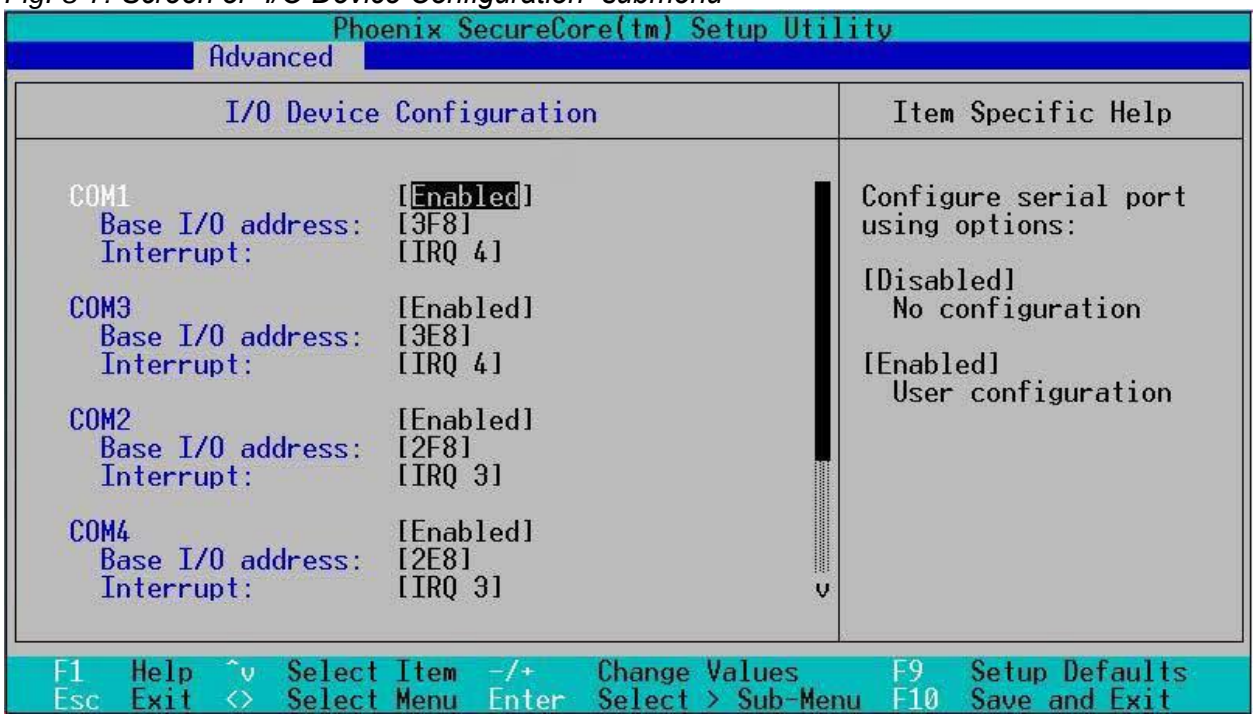
PCI/PNP ISA IRQ Resource Exclusion

Reservation menu of certain interrupts for the use by ISA bus devices. While opening this submenu, several interrupt request lines will be displayed and values [Available] or [Reserved] can be set for each separate line, where:
[Available] – is an interrupt available for PCI and embedded devices of the module
[Reserved] – is an interrupt reserved for ISA bus.

8.4.3. I/O Device Configuration

On the figure below shows the screen of “I/O Device Configuration” submenu.

Fig. 8-7: Screen of “I/O Device Configuration” submenu



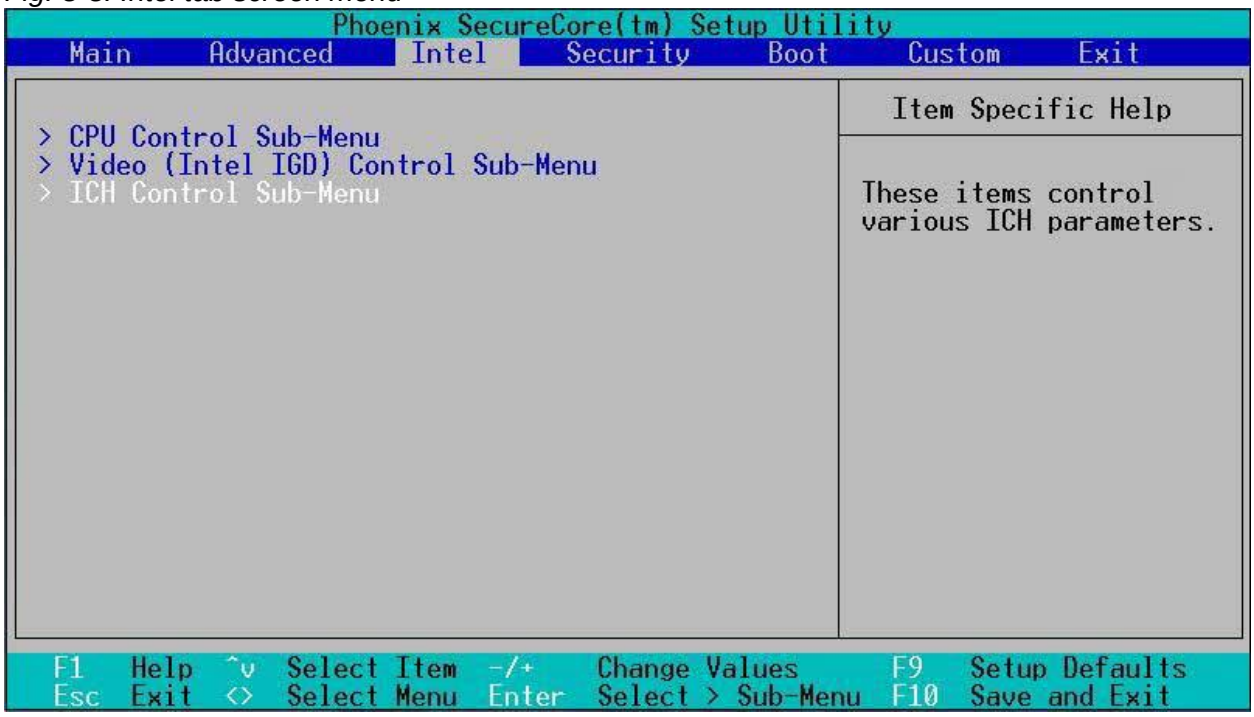
Where:

COM1 – **COM4** – set the parameters of RS232 port.

8.5. Intel

In this tab it is possible to make microprocessor and Intel chipset settings. The figure below shows the Intel tab menu.

Fig. 8-8: Intel tab screen menu

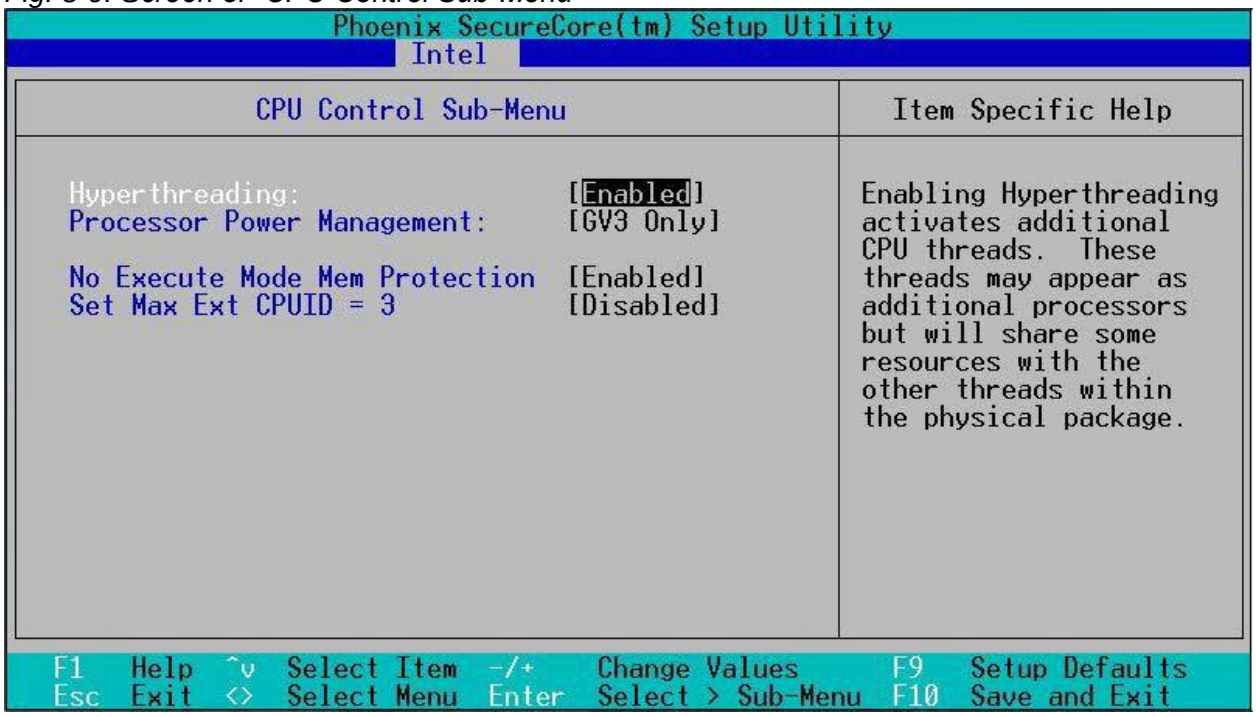


This tab's menu has several additional submenus.

8.5.1. CPU Control Sub-Menu

Submenu of CPU parameters control. This submenu is shown on the figure below.

Fig. 8-9: Screen of "CPU Control Sub-Menu"



Where:

Hyperthreading: - is a control of the CPU Hyperthreading mode

Processor Power Management: - settings of the CPU Power Management algorithm.

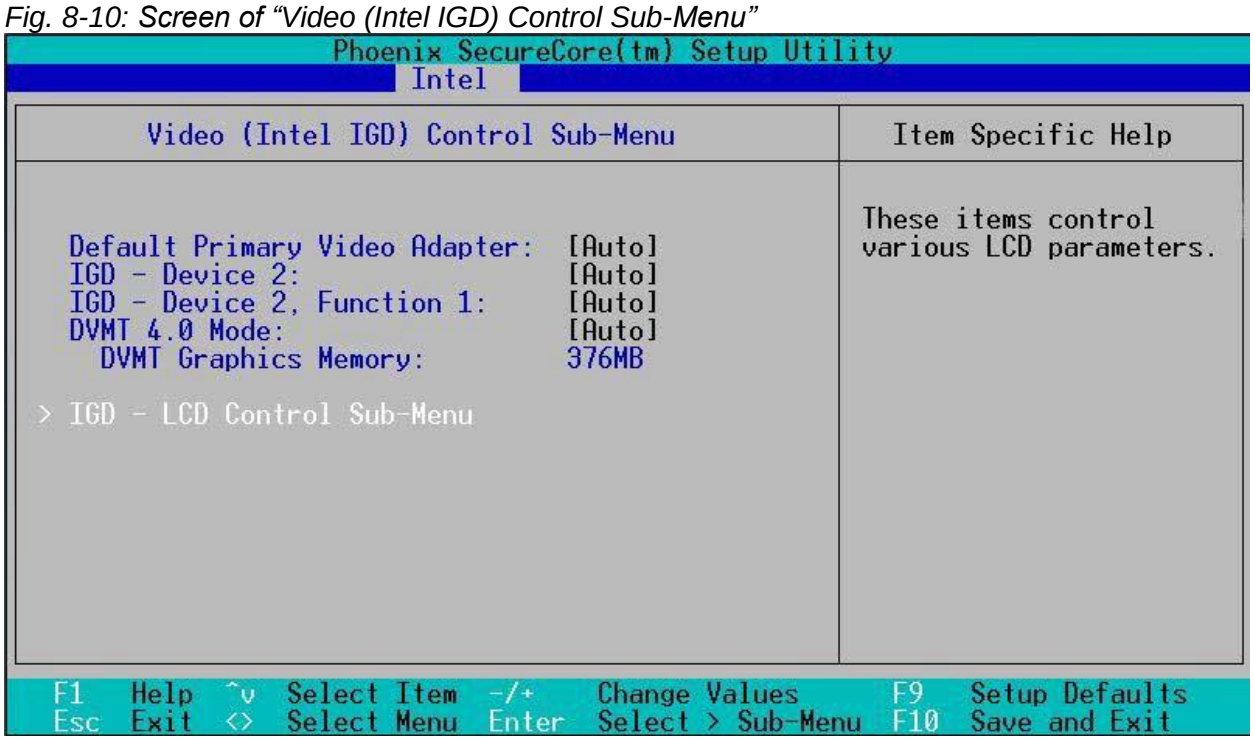
No Execute Mode Mem Protection – use the mechanism of data memory block protection against the executable code (Intel NX bit). Switched on by default.

Set Max Ext CPUID = 3 – setting maximum value for CPU ID (for support of old operating systems)

8.5.2. Video (Intel IGD) Control Sub-Menu

Submenu of control over the embedded video adapter parameters. This submenu is shown on the figure below.

Fig. 8-10: Screen of "Video (Intel IGD) Control Sub-Menu"



Where:

Default Primary Video Adapter: Selection of the primary video controller

[Auto] – Automatic adjustment

[IGD] – Integrated Graphics Device

[PCI] – External PCI video controller

IGD - Device 2: Control over the integrated video controller

IGD - Device 2, Function 1: Control of LVDS-output of the integrated controller

DVMT 4.0 Mode: Control of "Dynamic video memory technology" mode

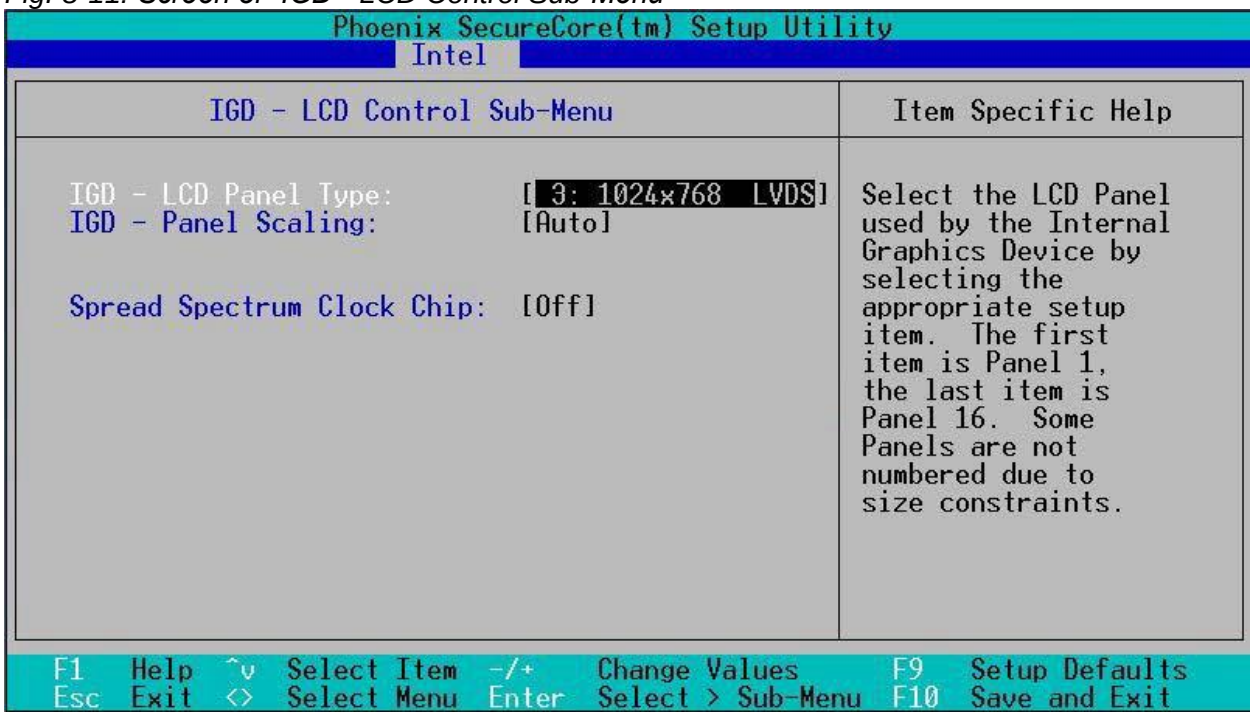
DVMT Graphics Memory: Adjustment of memory capacity dedicated for the integrated video controller

This submenu also contains another submenu for setting the parameters of LCD-panel connected to module via LVDS-interface.

8.5.2.1 IGD – LCD Control Sub-Menu

Submenu for setting the parameters of LCD-panel is shown on figure below.

Fig. 8-11: Screen of "IGD - LCD Control Sub-Menu"



This submenu has the following purpose:

- It enables to set the parameters of LCD-panel connected to the module via LVDS-port;
- Makes it possible to assign zooming.

8.5.3. ICH Control Sub-Menu

Submenu of control over the integrated chipset controllers. Screens of “ICH Control Sub-Menu” and “Integrated Device Control SUB-Menu” are shown on the figures below.

Fig. 8-12: Screen of “ICH Control SUB-Menu”

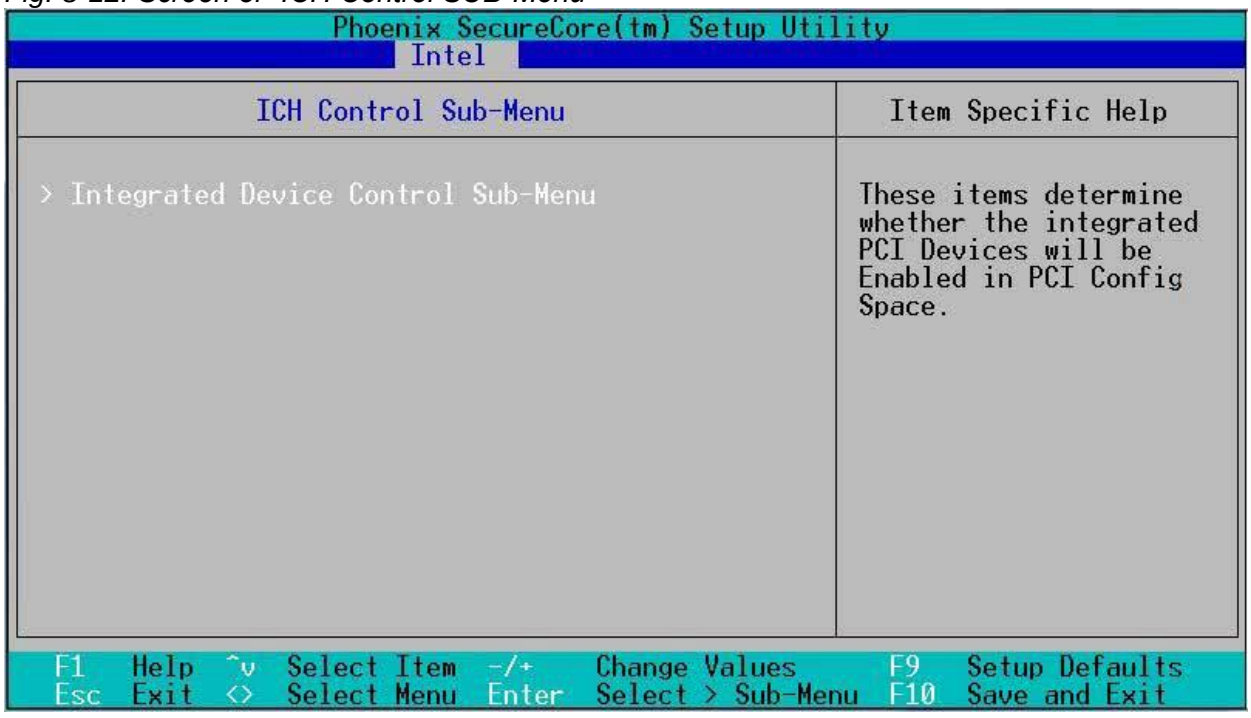
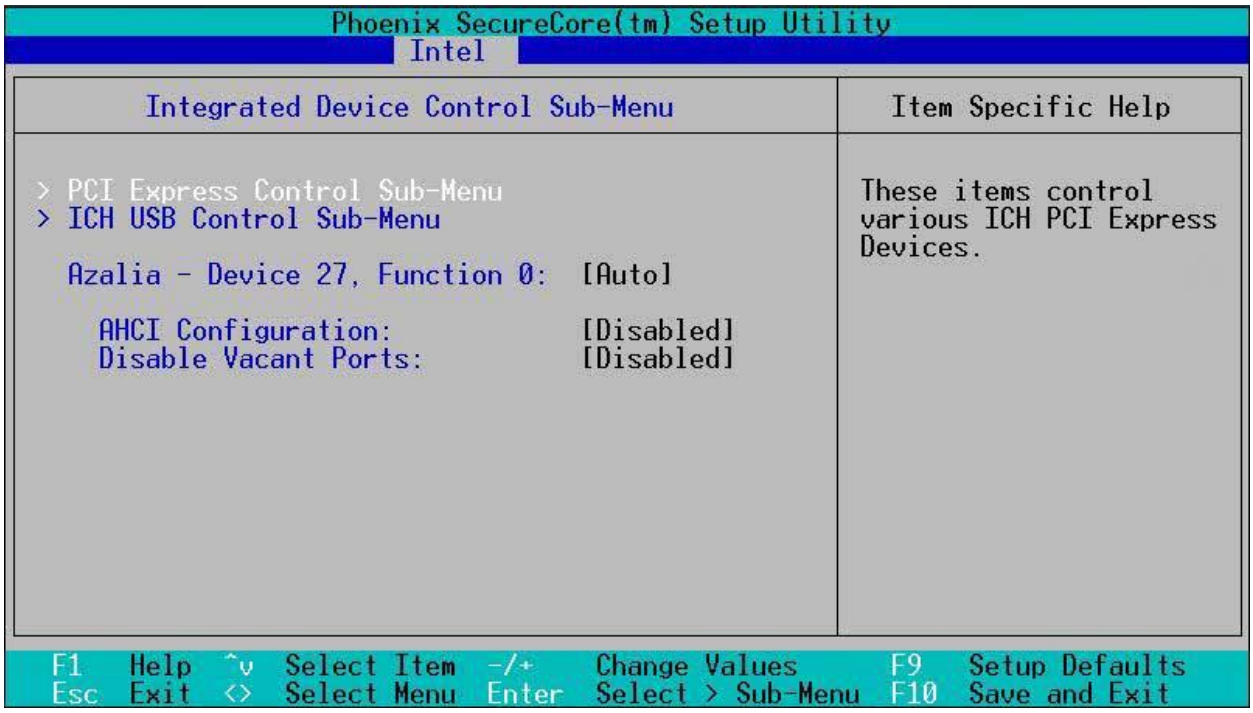


Fig. 8-13: Screen of “Integrated Device Control Sub-Menu”



Where:

Azalia - Device 27, Function 0: Control of integrated audio controller “Azalia”

AHCI Configuration: Control of AHCI-mode for SATA-devices

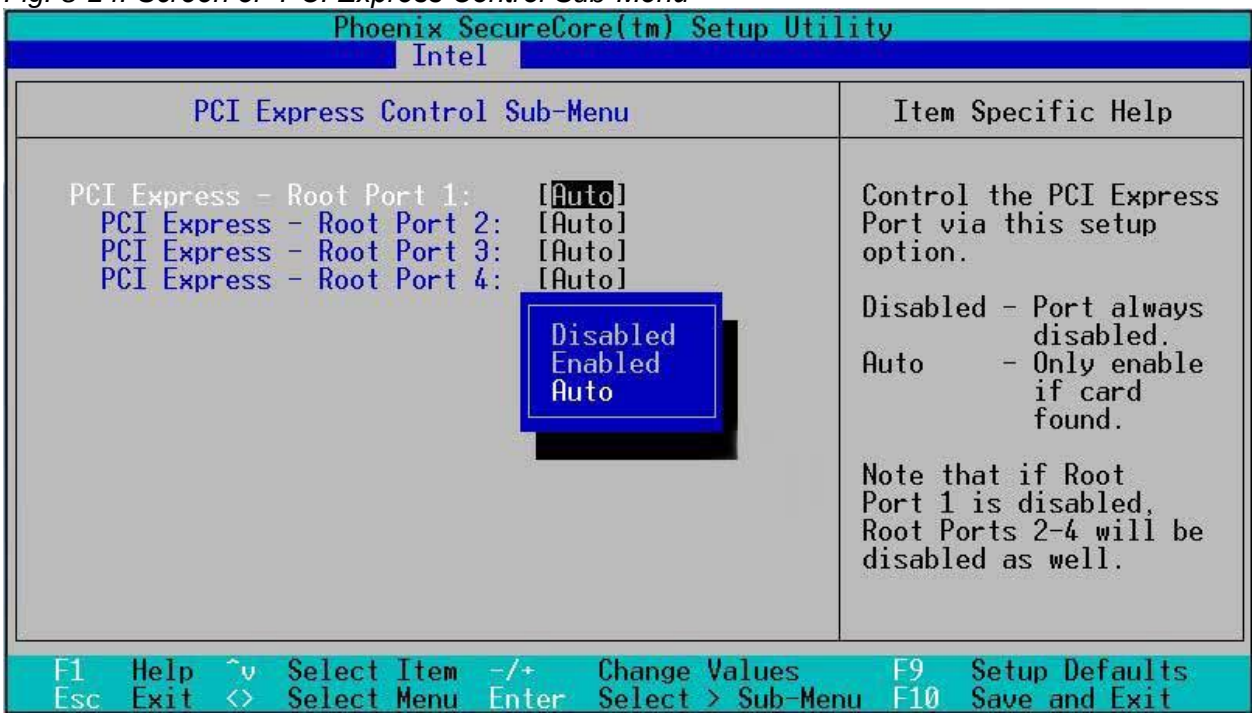
Disable Vacant Ports: Control of automatic shutdown of free SATA-ports.

This submenu also contains several more submenus.

8.5.3.1. PCI Express Control Sub-Menu

Submenu of control over PCI Express ports of the module. This submenu is shown on the figure below.

Fig. 8-14: Screen of “PCI Express Control Sub-Menu”



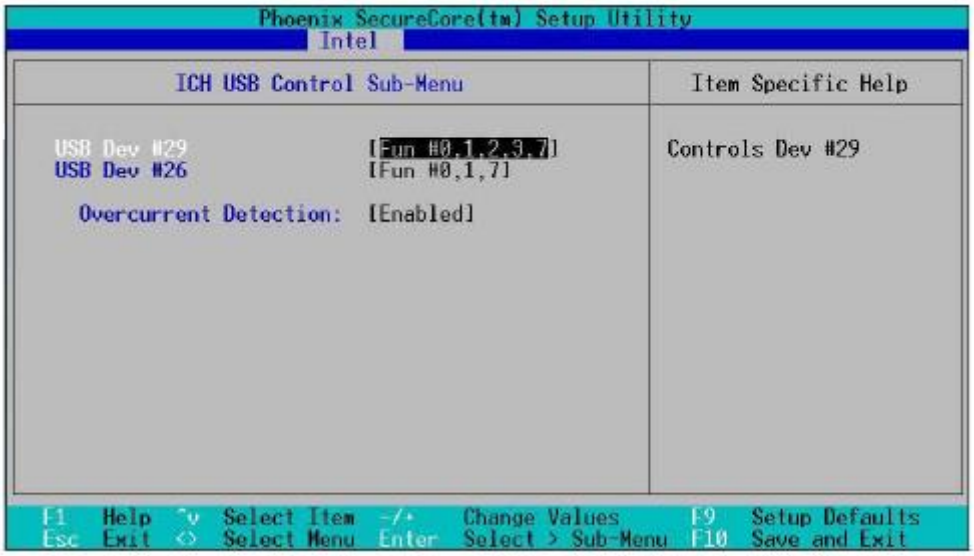
Where:

PCI Express – Root Port (1,2,3,4): Control of PCI Express port.

8.5.3.2. ICH USB Control Sub-Menu

Submenu of USB devices control. This submenu is shown on the figure below.

Fig. 8-15: Screen of "ICH USB Control Sub-Menu"



Where:
USB Dev #29, USB Dev #26: control over integrated USB-ports.
Overcurrent Detection: permission of interrupt generation in case of overcurrent via one of USB-ports.

8.6. Security

This tab is designed for the setting of module's protective functions. This tab is shown on the figure below.

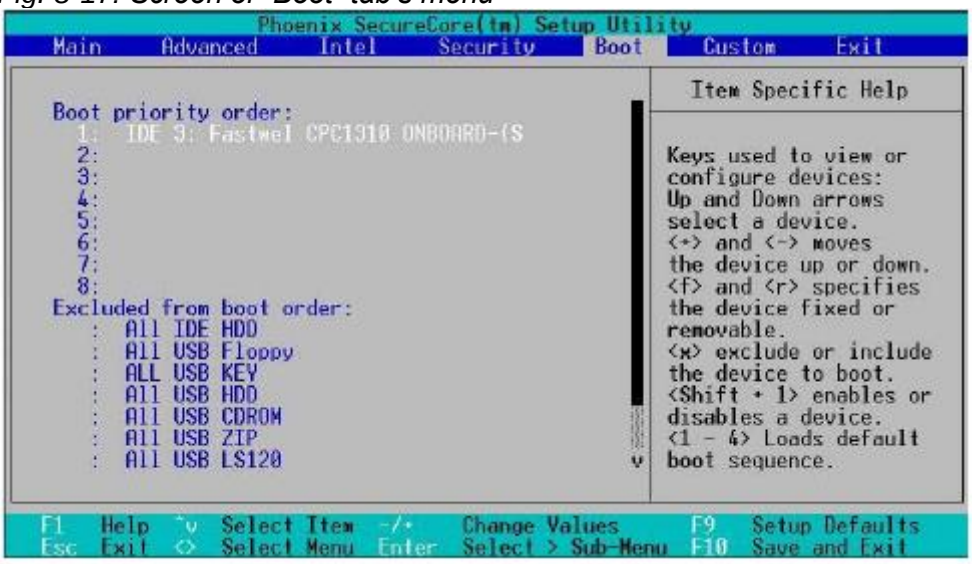
Fig. 8-16: Screen of "Security" tab submenu

Where:
Set Supervisor Password: is the setting of BIOS Setup password
Set User Password: Setting a password for module's start and entering to BIOS Setup
Fixed disk boot sector: Recording protection control for the fixed disc boot sector.
Virus check reminder: User reminder during BIOS POST of the fact that it is necessary to check the system for viruses.
Password on boot: Control over the password on boot (see Set User Password).

8.7. Boot

Tab for the setting of module's boot devices. This tab's submenu is shown on the figure below.

Fig. 8-17: Screen of "Boot" tab's menu

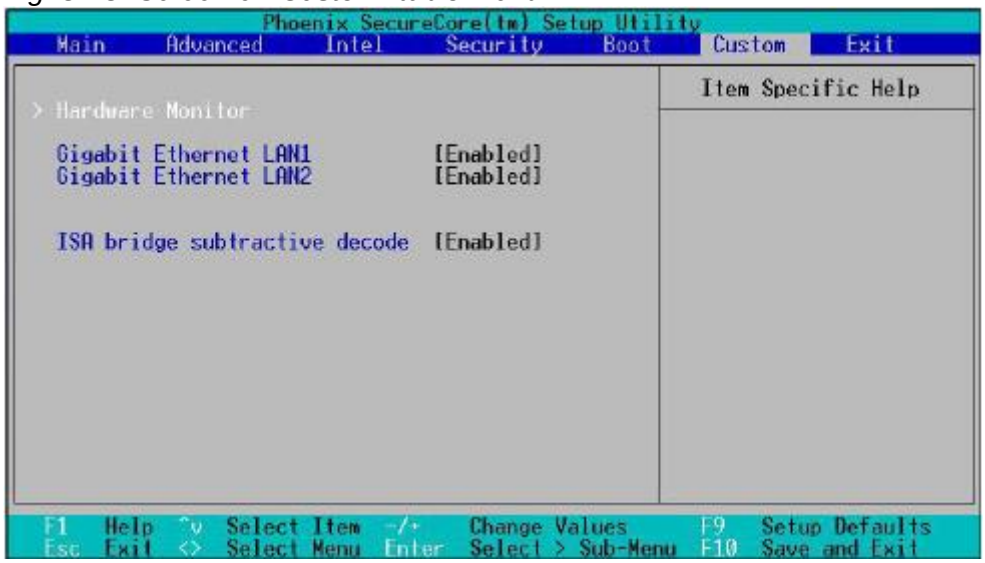


Where:
Boot priority order: is a setting of module's boot order from devices (devices can be selected via arrow keys, moving up and down – via "+" and "–" keys, deleting out from or entering into the list – via "x" key)

8.8. Custom

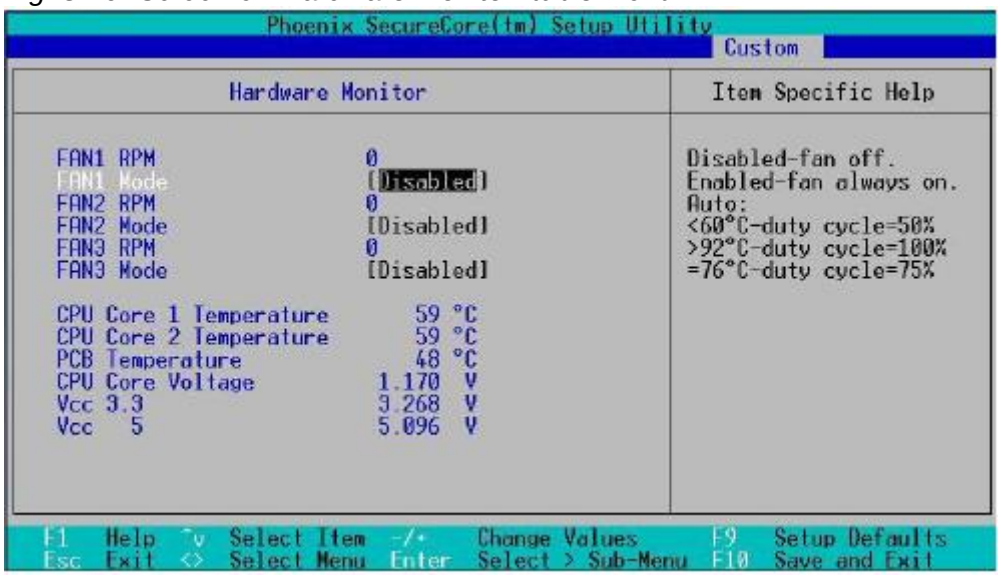
Menu of custom settings. This tab's menu is shown on the figure below.

Fig. 8-18: Screen of "Custom" tab's menu



"Hardware Monitor" submenu is shown on the following figure.

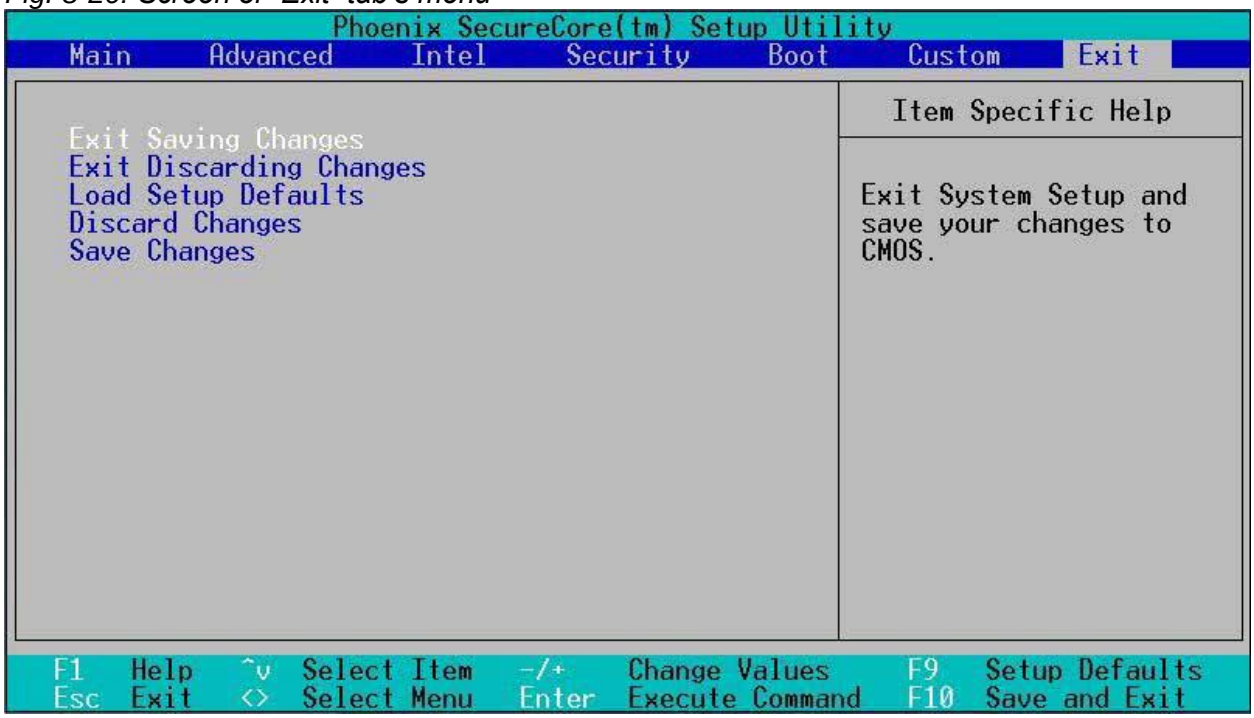
Fig. 8-19: Screen of "Hardware Monitor" tab's menu



8.9. Exit

Tab of BIOS Setup exit parameters. This tab's menu is shown on the figure below.

Fig. 8-20: Screen of "Exit" tab's menu



Where:

Exit Saving Changes: Exit from BIOS Setup with changes saved

Exit Discarding Changes: Discard changes and exit from BIOS Setup

Load Setup Defaults: -

Discard Changes: Discard changes made after opening BIOS Setup

Save Changes: -

Annex A

A. Recommendations for cooling system development

This section contains recommendations which should be considered by users while developing their own cooling systems. CPU can operate with maximum performance without passing over to the lower-power mode and reducing temperature, temperature of the heat-spreader should not exceed Tcase_max, values specified below:

CPC1310 – 01(-02) Tcase_max=88°C when Tamb=75°C

CPC1310 – 03(-04) Tcase_max=88°C when Tamb=80°C

(**T**amb – *ambient temperature, ° C*)

Therefore if a cooler of the heat-spreader maintains its temperature at a level not exceeding the specified limit temperature, CPU will operate in the maximum performance mode.

If heat-spreader temperature exceeds the limit temperature, CPU lacks sufficient cooling and passes to the reduced performance mode, which results in reduction of CPU operating frequency.