



# CPC152 MicroPC Vortex86DX™ 600 MHz CPU Module

# **User Manual**

Version 1.04

September 2015



The product described in this manual is compliant with all related CE standards.

Product Title: CPC152

Document name: CPC152 User Manual Manual version: 1.04 Copyright © 2015 Fastwel Co. Ltd. All rights reserved.

#### **Revision Record**

Rev. Index	Brief Description	Product Index	Date
0.01	Item number: 687263.045 v.1.0 Initial version of User Manual CPC152	CPC152	July 2013
1.00	Item number: 687263.045 v.1.1Section 2.8"Description of internal registers": description of control registers / interrupt state is added by new information, description of control register of page access to NV SRAM 128KBSection 1.6"Location of components and external view of 	CPC152	December 2013
1.01	Item number: 687263.045 v.1.1 Section 1.10.22 "Audio port" – recommendation for switching jumpers on KIB98102 interface module has been adjusted. New Section 2.8.3 "Register of interrupts state of ISA bus controller". Section 2.8.5 "Registers of interrupts control of ISA bus controller" – purpose of interrupt control bits has been changed. Section 5.3 "PCI/ PnP (Additional PCI plug and play settings)" – table of additional settings description has been supplemented by a section, connected to the SYSTEM_EVENT. Section 1.10.8 "IDE (XP16) port" is supplemented with recommendations for the connection of external IDE devices and a table of possible combinations of external and internal IDE (Master/Slave) devices. Section 5 "Basic Input/Output System (BIOS)" is supplemented with new information in accordance with the changes in the new module's version (subsections are added with the description of purpose of interrupt line integrated devices).	CPC152	April 2014
1.02	Section 1.6         "Location of components and CPC152 external view"         CPC152         April 2014           - scheme with the location of module's major components has been updated.         CPC152         April 2014		April 2014
1.03	Section 1.9 "Additional equipment" – obsolete devices were deleted from the list.	CPC152	April 2014
1.04	<u>Section1.9</u> "Additional equipment" has been added with Compact Flash MIC23012 (64 GB). <u>Section 1.10.7</u> "Compact Flash (XP1)" has been added with a table of compatibility with Compact Flash MIC230xx modules.	CPC152	June 2014

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Fastwel welcomes suggestions, remarks and proposals regarding the form and the content of this Manual.

This manual contains technical description, regulations, directions and recommendations for installation, setting and operation of CPC152 CPU module, manufactured by Fastwel.

CPC152 CPU module is designed for the use as part of various integrated systems, which require a combination of high performance and a low level of heat power released and power consumption, operation within an extended temperature range (-40...+85°C), as well as compatibility of applications with x86 architecture of CPUs. CPC152 is implemented in MicroPC format and is compatible with the majority of peripheral modules and power sources, supplied by various manufacturers.

The document is designed for developers of distributed control and data acquisition systems, for IT administrators and engineers in industrial automation area.

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# NOTATIONS



# Attention, high voltage!

This sign and caption warn you about the dangers, related to electric discharges (> 60 V) when touching a product or any parts thereof. Failure to observe safety measures, mentioned or prescribed by the regulations, may expose your life or health to danger, as well as may lead to product damages. See also the section, devoted to operation with a high voltage, specified below.



#### Attention! Device, sensitive to static electricity!

This sign and caption indicate that electronic boards and their components are sensitive to static electricity. This is why it is required to exercise caution when handling this device and and at the time of inspections, in order to guarantee integrity and working capacity of the device. See also Section, devoted to the directions for handling with the board and unpacking, specified below.



# Attention! Hot surface!

This sign and caption warn us of a danger, related to touching hot surfaces, containing within the device.



# Attention!

This sign is designed to make you consider those aspects of the User Manual, which incomplete understanding or failure to follow could endanger your health or result in damages of the equipment.



# Note

This sign is used to mark the parts of the text, which should be read thoroughly.

# Safety requirements

This product is designed and tested for the purpose of ensuring compliance with the electric safety requirements. Its design guarantees long-term failsafe operation. Life cycle of the device can be sufficiently reduced due to improper handling during unpacking and installation. Therefore, for your own safety and in order to ensure the proper operation of the device, you should observe the below recommendations.

# High-voltage safe handling rules



# Attention!

All works with this device should be performed only by employees which have sufficient skills for these types of works.



# Attention, high voltage!

Before installing the board into the system make sure that the mains supply is off. This also applies to installation of extension boards.

During installation, repairs and maintenance of the device, there is a serious risk of electric shock, this is why you should always unplug the power cord from the socket during carrying out of works. This also applies to other feeder cables.

# **BOARD HANDLING INSTRUCTIONS**



# Device, sensitive to static electricity!

Electronic boards and their components are sensible to static electricity. This is why you should give special attention to handling with these devices in order to ensure their integrity and working efficiency.

Do not leave the board without protective packaging, when it is not operated.

When applicable, always operate the board at the workplace equipped with protection against static electricity. If it is impossible, the user should remove a static discharge before touching the device by hand or using tools. The best way to do it is touch a metal part of system enclosure.

Crucially, the safety precautions should be observed during operations related to the replacement of jumpers etc. If the device is equipped with batteries for power supply of memory or real-time clock, do not put the board onto current conducting surfaces, such as antistatic mats or sponges. They could cause short circuit and lead to damages of battery and board conducting circuits.

# **General Board Operation Rules**

- To preserve the manufacturer's guarantee, the product must not be reworked or altered in any way. Any alterations and improvements not authorized by Fastwel Group Co. Ltd company, except those described in this Manual or obtained from the Fastwel Group Co. Ltd technical support service in the form of a set of instructions describing their performance cancel the guarantee.

- This device must be only installed into and connected to systems meeting all necessary technical and climatic requirements. This relates to the operating temperatures range of the specific board design version. The temperature limitations of the batteries installed on the board should be taken into account as well.

- Please follow only the instructions of this Manual while performing all necessary installation and configuring operations.

- Keep original package to store the product in the future or to transport it in case of a guarantee event. Should it become necessary to transport or store the board, pack it in the same way it was packed upon receipt.

- Take particular care during handling the product and its unpacking. Act in accordance with the instructions of the above section and Chapter 6 6. TRANSPORTATION, UNPACKING **AND STORAGE** 

# The Manufacturer's Guarantees

# Guarantee Liabilities

The Manufacturer hereby guarantees the product conformity with the requirements of TU 4013-004-52415667-05 specifications, provided the Consumer abides by the conditions of operation, transportation, storage, installation and assembly established by the accompanying documents.

The Manufacturer hereby guarantees that the products supply thereby are free from defects in workmanship and materials, provided operation and maintenance norms were observed during the currently established guarantee period. The Manufacturer's obligation under this guarantee is to repair or replace free of charge any defective electronic component being a part of a returned product.

Products that broke down through the Manufacturer's fault during the guarantee period will be repaired free of charge. Otherwise the Consumer will be invoiced as per the current labor remuneration rates and expendable materials cost.

# **Liability Limitation Right**

The Manufacturer shall not be liable for the damage inflicted to the Consumer's property because of the product breakdown in the process of its utilization.

# **Guarantee Period**

The guarantee period for the products made by the manufacturer company is 36 months since the sale date (unless otherwise provided by the supply contract).

The guarantee period for the products made to special order is 60 months since the sale date (unless otherwise provided by the supply contract).

# The warranty set forth above does not extend to and shall not apply to:

User Manual CPC152 Specification
----------------------------------

- 1. Products, including software, which have been repaired or altered by other than Fastwel personnel, unless Buyer has properly altered or repaired the products in accordance with procedures previously approved in writing by Fastwel.
- 2. Products, which have been subject to power supply reversal, misuse, neglect, accident, or improper installation.

# Returning a product for repair

- 1. Apply to Fastwel company or to any of the Fastwel's official representatives for the Product Return Authorization.
- 2. Attach a failure inspection report with a product to be returned in the form, accepted by customer, with a description of the failure circumstances and symptoms.

3. Carefully package the product in the antistatic bag, in which the product had been supplied. Failure to package in antistatic material will VOID all warranties. Then package the product in a safe container for shipping.

4. The customer pays for shipping the product to Fastwel or to an official Fastwel representative or dealer.

# **SECTION 1**

# **BRIEF DESCRIPTION**

# **1 BRIEF DESCRIPTION**

# 1.1 Device purpose

CPC152 CPU Module is a high-integrity solution based on x86 platform in MicroPC format, designed for use in real-time management, manufacturing control as well as data collection and processing systems. The module can operate in an independent or slave mode.

Connection of primary I/O devices (VGA displays, TFT-panels, AT-keyboards and other handling equipment, audio devices, printers USB devices) makes it possible to use the CPC152 CPU Module in the systems attended by operator. For storing data it is possible to use both an integrated drive and external USB and IDE devices.

In addition to the standard MicroPC extension bus (ISA 8-bit), the module is equipped with PC/104 bus (ISA 8/16-bi), which makes it possible to connect extra extension modules to CPC152.

CPC152 can be connected to RS-232, RS-422/485, Ethernet networks, which enables to use the module in distributed I/O and data processing systems.

# **1.2 General information**

- CPU: Vortex86DX<sup>™</sup> 600MHz
  - 32 bit x86 core
  - 16 bit memory bus
  - L1 Cache (32 KB)
  - L2 Cache (256 KB)
  - System bus frequency 333 MHz
- RAM:
  - soldered DDR2 SDRAM 256 MB
- Flash-drive:
  - PATA NAND Flash controller with integrated system of ECC control and wear
  - 2 GB NAND Flash (SLC)<sup>1</sup>
- FLASH BIOS:
  - 256 KB modifiable within the system and back-up copy
  - Automatic switching to the backup copy in case of error when booting the primary copy
  - Integrated nonvolatile memory:
    - Internal memory 256 byte
    - 8 KB FRAM (SPI), used for storing configuration, calibration factors of sensors
    - 128 KB SRAM (ISA)
       Consumption current from 3 V battery, when the power is OFF: 4 mkA<sup>2</sup> consumption current from 3V battery when the power is ON: 2 mkA<sup>3</sup>

<sup>&</sup>lt;sup>1</sup> Available volume of integrated drive: 1.8 GB

<sup>&</sup>lt;sup>2</sup> Standardized value under normal conditions (humidity from 5 to 95%, +25°C).

<sup>&</sup>lt;sup>3</sup> Standardized value under normal conditions (humidity from 5 to 95%, +25°C).

- Extension buses:
  - MicroPC (ISA 8-bit, 8/16 MHz)
  - PC/104 (ISA 8/16-bit, 8/16 MHz)
- Connector for Compact Flash:
  - Support of Type 1 / 2 modules
  - support of PIO, DMA, UDMA modes
- Port of HDD connection:
  - 1x Primary channel
  - Connection up to 2x devices
  - Support of Ultra-DMA 100
- Port LAN 10/100 Mb:
  - Standard RJ45 connector with LED indication
  - Insulation from the system: 500 V
- USB ports (host):
  - Support of USB 1.1, USB 2.0 (HS, FS, LS)
  - Connection up to 4-x devices
  - Standard connector 2x USB Type A
- Video subsystem:
  - Video controller with 2D accelerator
  - Volume of video memory: 16 MB DDR
  - Independent connection of 2x displays
  - Port for the connection of RGB display with resolution up to 1920x1440, 32 bit color
  - Port for the connection of TFT-panels with resolution of up to 1920x1440, 18 bit color
  - Connection of display via a separate VGA (connector XP2, IDC2-10) port.
  - Connection of the display via a standard connector DSUB15F using KIB98102 interface board
- Audio port:
  - Linear stereo input/output:
  - Input for MIC connection (mono)
- Universal parallel port with support of SPP, EPP, ECP modes
  - Connection via a separate IDC-26
  - Connection of devices via standard DSUB-25 connector, using KIB98201 interface board
- Serial ports:
  - COM1: isolated RS-422/485 (individual insulation form the system: 500 V)
  - COM2: isolated RS-422/485 (individual insulation form the system: 500 V)
  - automatic (hardware) control of information transfer direction for RS-422/485 ports
  - COM3: RS-232 (9-wore, full set of signals)
  - COM4: RS-232 (9-wore, full set of signals)
  - exchange rate via RS-232 up to 250 KB/sec
  - exchange rate via RS-422 / RS-485: up to 750 KB/sec<sup>4</sup>
  - ESD protection: 15 kW (IEC1000-4-2)

<sup>&</sup>lt;sup>4</sup> Exchange rate via serial ports is defined by a frequency divider register value.

- GPIO port:
  - 8x lines (compatible with 5 V)
  - GPIO\_P2[7:0] CPU port is used
  - Maximum output load capacity: 16 mA
  - compatibility with 5 V level
  - using the port for control of servo drives (PWM)
  - ability to use the port in the mode of compatibility with 8051
- PS/2 keyboard and mouse port
- Watchdog timers:
  - two watchdog timers, integrated into CPU, with a programmable event and actuation interval of 30.5 microseconds...512 seconds
  - One watchdog timer, integrated into the power supply supervisor, with a fixed actuation interval of 1.6 seconds
- Real-time clock
  - Consumption current when the power is OFF: 2 mkA<sup>5</sup>
- Integrated lithium battery of 3 V (CR2032, standardized capacity 180...220 mA•h)
- Opto-isolated reset / interrupt
  - Potential-free contact
  - Voltage 3...15 V, 10...30 V
- Generation of interrupt / reset in case power supply voltage is lower than 4.65 V
- PC buzzer
- Temperature sensor (LM92, 55 ...+ 125° C)
- Digital accelerometer (measuring acceleration via 3 axes)
- Digital barometer (measuring pressure from 50 to 115 KPa)
- Compatibility with operating systems: <sup>6</sup>
  - FreeDOS, Microsoft<sup>™</sup> MS-DOS® 6.22
  - Linux 2.6
  - Microsoft™ Windows CE 5
  - Microsoft<sup>™</sup> Windows XP Embedded
  - QNX 4.25, QNX 6.5x
- Console ports: COM3/4 and/or VGA/TFT and/or Keyboard
- Extension buses:
  - ISA 8 bit (MicroPC)
    - ISA 8/16 bit (PC/104)
- Power supply voltage: +5 V ± 5%
- Consumed current (without external devices):
  - no more than 0.85 A @ 5 V (at +25°C)

 $<sup>\</sup>frac{5}{2}$  Standardized value under normal conditions (humidity from 5 to 95%, +25°C).

<sup>&</sup>lt;sup>6</sup> By default, the module is supplied with preinstalled FreeDOS.

- Operating temperature range: from 40 to + 85° C
- Modules storage conditions 1 in accordance with GOST 15150-69
- Humidity: up to 95%, at +25°C without condensation
- Resistance to multiple shocks: 50g
- Vibration resistance: 5g
- MTBF: No less than 160 000 hours
- Dimensions: 125.0 × 123.0 × 27.0 mm (no more than)
- Module weight: No more than 140 g (without CompactFlash card)

# 1.3 Connection to module

Below is a standardized list of interface boards and devices, which could be connected to CPC152:

- Devices with Ethernet 10 / 100 Mb/sec interface
- RS-232 compatible devices
- RS-422 / RS-485 multiuser networks
- Compact Flash type 1 / 2
- 2.5" and 3.5" HDD (PATA interface, via KIB98201)
- USB devices, types 1.1 and 2.0 (Full-speed, High-speed), including devices of USB Mass Storage Device type
- Floppy Disc Drive (only USB port)
- Keyboard, mouse controller (ports PS/2, USB)
- LCD panels (digital RGB), via KIB98102 or via XP2 connector
- VGA displays and TFT-panels (analog RGB)
- Audio devices (via KIB98102)
- PC-compatible printer (ports USB, LPT)
- Other modules in MicroPC (ISA 8 bit) and PC/104 (ISA 8/16 bit) formats graphics cards, additional memory cards, digital / analog I/O modules, communication/special-purpose modules etc.
- Isolated reset / interrupt signal

# 1.4 Module power supply

Module's electric power supply should correspond to the requirements, specified in the table 1-1. Module is supplied with power via MicroPC and PC/104 connectors.

In addition, for transferring power supply voltage from an external source there is additional XP20 power supply connector (4- pin connector Molex 22-27-2041). As a mating part, it is recommended to use 22-01-2047 (Molex) connector – 1 pcs., contacts 08-52-0101 (Molex) – 4 pcs. The kit, containing socket and contacts for the connection of power supply via additional connector – ACS00039.

Power supply source should provide starting current, specified in the table below, depending on module's version. It is also permissible to use a power supply source with a current limitation mode of no less than 2.0 A. When choosing the power supply source, consideration should be given to the starting current of CPC152 and consumption current of extension modules and other devices connected to the ports of CPC152.

The module is equipped with a "soft" start mechanism, enabling to reduce the maximum value of starting current during the voltage supply. Module's start delay after voltage supply amounts to 200 msec approx. (no more than). Additional measures should be taken, in order to provide particular level on lines of I/O ports within a period of 200 msec after power supply.

Version	Power supply voltage, V	Operating range of power supply voltages, V	Load current, A	Starting current, A
CPC152-01	+5	from +4.75 to +5.25	2.0	2.5

#### Table 1-1: Requirements to parameters of the power supply source

# 1.5 Block diagram of CPC152



#### Fig. 1-1: Block diagram of CPC152

# 1.6 Location of components and external view of CPC152



CPC152



Fig. 1-3: Location of primary components of CPC152



Purposes of module's connectors are described in section 1.9 Integral parts of CPC152 and in section 2.9 Tables of module's connectors contacts.

Purpose of X1...X40 switches is given in section 3.1 Setting module's switches.

# 1.7 Versions

CPC152 is supplied as one version:

CPC152-01 – CPU Module CPC152 (MicroPC), Vortex86DX 600 MHz, 256 MW DDR2 SDRAM, GPU SM718 (16 MB DDR), 2 GB FFD, NV SRAM 128 KB, Compact Flash socket, 4 x USB 2.0, Ethernet 10/100 Mbps, 2 x RS-232, 2 x RS-422/485 (isolated, with lightning protection); acceleration, pressure and temperature sensors.

# Additional options for CPC152-01:

Preinstalled operating system		
\WCE	Windows CE 5.0	
\LNX	Linux 2.6	
\WXPe	Windows XP Embedded	
Coating		

\COATED	Conformal coating			
41 C ()				

\* Information on possibility of pre-installing QNX operating system is provided upon special request.

# **1.8 Delivery checklist**

Standard delivery checklist for CPC152 includes:

- 1. CPC152 Module;
- 2. Cable adapter ACS00005-01 (port RS-232, IDC-10 / DB9M, length 180 mm);
- 3. Cable adapter ACS00027-02 (port VGA, IDC2-10 / D-SUB 15F, length 180 mm);
- 4. Removable part of the terminal block WAGO 733-105 (port RS-422/485), 2 pcs.;

cable adapter IDC-10 / D-SUB 9F (port RS-232, length 1800 mm)

- 5. Set of jumpers (step 2);
- 6. Package.

# 1.9 Additional accessories

KIB98102 KIB98201	Interface board (Audio, VGA, TFT, PS/2) Interface board (2.5" HDD, 3.5" HDD, LPT)
ACS00015	cable adapter for KIB98102 (length 300 mm)
ACS00015-01	cable adapter for KIB98102 (length 120 mm)
ACS00015-02	cable adapter for KIB98102 (length 140 mm)
ACS00015-03	cable adapter for KIB98102 (length 500 mm)
ACS00016	cable adapter for KIB98201 (length 300 mm)
ACS00016-01	cable adapter for KIB98201 (length 120 mm)
ACS00016-02	cable adapter for KIB98201 (length 140 mm)
ACS00016-03	cable adapter for KIB98201 (length 500 mm)
ACS00005	cable adapter IDC-10 / D-SUB 9M (port RS-232, length 1800 mm)
ACS00005-01	cable adapter IDC-10 / D-SUB 9M (port RS-232, length 180 mm)

ACS00006

ACS00010 ACS00027-02 ACS00042 ACS00043 ACS00051-01 ACS00058 ACS00031-02 ACS00031-03 ACS00039 ACS00064 ACS00064-01	FC44 – 2.5" HDD, connecting cable cable IDC2-10 / D-SUB 15F (port VGA, length 180 mm) null modem cable 1.8 m cable adapter PS/2 (PHR-6 / MiniDIN-6F) cable adapter 2x USB Type A Female (2x USB ports) kit of Li battery 3 V with PHR-2 connector (length 40 mm) PHR-6 socket with contacts (port PS/2) PHR-2 socket with contacts (RESET, PC-Speaker, VBAT ports) Molex 22-01-2045 socket with contacts (additional power supply connector) connector for ribbon cable 89947-710LF (VGA, GPIO, USB ports) connector for cable 10073599-020LF, FCI with contacts (VGA, GPIO, USB ports)
ICC19001	ISA-8 mounting frame MicroPC, 4 slots
ICC19101 ICC19201	ISA-8 mounting frame MicroPC, 8 slots ISA-8 mounting frame MicroPC, 12 slots
ICC19301	ISA-8 mounting frame MicroPC, 3 slots, desk-mounted
ICC19401	ISA-8 mounting frame MicroPC, 6 slots, wall-mounted
PS151-01	Power supply source: 5V/6A, 12V/1.6A, 3.3V/3A, isolation input/output 1500V, control system, UPS function
AIC324-01	Analog digital input/output module AIC324 PC104 analog-to-digital converter 16bit/32 channels/250kHz/±10V ±0.625V, Digital-to-analog converter 16bit/6µs/4 channels/±10V ±2.5V, 24 digital inputs/outputs, timer 32/16 bit, -40+85C
AIC324-02	Analog digital input/output module AIC324 PC104 analog-to-digital converter 16bit/32 channels/250kHz/±10V ±0.625V, Digital-to-analog converter 16bit/6µs/4 channels/±10V ±2.5V, 24 digital inputs/outputs, timer 32/16 bit, -40+85C, high precision
MIC23003	CompactFlash drive, 128 MB, -40°C+85°C
MIC23004	CompactFlash drive, 256 MB, -40°C+85°C
MIC23005 MIC23006	CompactFlash drive, 512 MB, -40°C+85°C CompactFlash drive, 1 GB, -40°C+85°C
MIC23007	CompactFlash drive, 2 GB, -40°C+85°C
MIC23008	CompactFlash drive, 4 GB, -40°C+85°C
MIC23009 MIC23010	CompactFlash drive, 8 GB, -40°C+85°C CompactFlash drive, 16 GB, -40°C+85°C
MIC23011	CompactFlash drive, 32 GB, -40°C+85°C
MIC23012	CompactFlash drive, 64 GB, -40°C+85°C

List of additional accessories on Fastwel ftp-server: <a href="http://ftp.prosoft.ru/pub/Hardware/Fastwel/ACSx/">http://ftp.prosoft.ru/pub/Hardware/Fastwel/ACSx/</a>

# 1.10 Constituent parts of CPC152

# 1.10.1 CPU

CPC152 module is based on x86-compatible 32-bit Vortex86DX CPU with low power consumption and manufactured using 90 nm technology. CPU clock frequency is 600 MHz. A more detailed information on the CPU, as well as latest versions of drivers and system-level software can be found at manufacturer's website: http://www.dmp.com.tw/tech/vortex86dx/.

# 1.10.2 Supervisor and watchdog timer

The CPU module contains power supply supervisor (microchip which monitors module's supply voltage), well as hardware watchdog power as 3 timers: 2 watchdog timers integrated into the CPU (WDT0, WDT1) and 1 external, integrated into power supply supervisor (WDT2). Supervisor generates RESET hardware signal when the power supply voltage "3.3V" drops lower than 3.08 V, as well as NMI signal / interrupt / hardware reset at the reduction of principal power supply voltage "5V" lower than level of 4.65 V, which enables to save user data in the nonvolatile RAM, if necessary. Permission for NMI generation during the reduction of power supply voltage lower than the level of 4.65 V is provided within the SYSTEM BIOS SETUP (see. Section 3.2 Module parameters configuration).

Watchdog timers can be used to avoid software hangups:

- Actuation of WDT0, WDT1 watchdog timers is performed when there are no software confirmations within 30.5 µs... 512 sec. Internal watchdog timer is launched in the SYSTEM BIOS SETUP. Actuation of internal watchdog timers is carried out without generation of RESET hardware signal.
- Actuation of WDT2 watchdog timer is carried out when there are no software confirmations within 1.6 sec approximately (within the whole temperature range: from 1.0 sec to 2.25 sec). External watchdog timer WDT2 has been launched after power ON or reset. Actuation of an external watchdog timer is carried out with generation of RESET hardware signal. WDT2 is switched off when the control is transferred to operating system. In case of jumper is installed, which enables automatic switching to BIOS back-up copy, then in case of an error during BIOS code execution, an automatic system reset and system boot from back-up copy will be carried out. In this case, BIOS Setup settings will be reset to default settings.



# Attention!

For CPC152, using an external watchdog timer WDT2 in application programs, it is required to turn OFF an automatic switching to the BIOS back-up copy (see Section 3.1.9 "Switching to BIOS booting from the primary/reserve source").

# 1.10.3 Random Access Memory (RAM)

As system memory, the module uses dynamic memory DDR2 SDRAM with a total volume of 256 MB. Bus operation frequency: 333 MHz.

No memory extension module is to be installed.

# 1.10.4 Nonvolatile memory (NV SRAM)

The module is equipped with integrated nonvolatile memory 256 byte for storage of configuration data (CMOS), recorded by **SETUP** program integrated into BIOS.

In addition, the use of integrated FRAM 64 KB or static nonvolatile memory of 128 KB is possible.

Line "GPCS0\_" of address decoder integrated into CPU is used for accessing static nonvolatile memory. For work with nonvolatile RAM it is required to install the relevant option in BIOS Setup settings, as well as install respective jumpers.

Access to the nonvolatile RAM – page-oriented, page size of 16 KB (page-oriented access to NV SRAM – in CPC152 modules, starting from version 1.1). The pages are switched by recording page numbers to I/O register, see. <u>Section 2.8.5 Control register of page-oriented access to NV SRAM 128KB.</u>

Base window address is selected in BIOS Setup settings (by default: D8000h). (see. <u>Section 5.6.2.5 "NV SRAM Configuration"</u>).



#### Attention!

For using nonvolatile RAM it is required to install X40 switch.

# 1.10.5 Read-only memory (FLASH BIOS)

In order to store Basic Input/Output System (hereinafter referred to as the BIOS), the module uses FLASH-memory microchip of 512 KB. It is also possible to boot from the BIOS backup copy, stored in the internal Flash-memory, integrated into Vortex86DX CPU microchip.

The module stores two BIOS copies – primary and backup copy.

CPC152 are equipped with a mechanism of automatic switching to BIOS backup copy. By turning the power ON, the module will be booted from primary BIOS copy. If an external watchdog is actuated, which is integrated into ADM706T power supply supervisor microchip, the module will be rebooted with a BIOS backup copy (for automatic reboot, it is required to install X8 jumper). If X8 jumper is not installed, the boot from the backup copy will be carried out only after manual hardware reset of the module (reset button or remote reset port).

If you want to boot only from the primary BIOS copy, it is required to install X1 jumper. If X1 jumper is installed, the module will not be switched to BIOS backup copy.

X1 jumper should also be installed if there is watchdog timer, WDT2 is used in the user program in order to avoid software failures with an automatic reboot of CPU at the end of a timeout of 1 sec. Flag of WDT2 watchdog timer actuation is available regarding reading of GPIO1[0] line: '0' – watchdog timer has been actuated, '1' – watchdog timer has not been actuated (flag value is snapped with a trigger and can be reset by recording '0' to the GPIO1[1] port and a further record '1'). This way enables to control the reason of hardware reset in case of watchdog timer actuation, even after reboot of the CPU.

In case of further actuations of the WDT2 external watchdog timer, the module will also reboot from the backup BIOS copy. Booting can be resumed from the main copy using one of the following three methods:

- By using a relevant item in BIOS Setup settings;
- By installing GPIO\_P3[7] line in '0';
- By turning OFF and turning ON of module's power supply.

Indication of watchdog timer actuation and indication of booting from the main BIOS copy is carried out using HL4 LED.

Hardware reset is indicated by HL3 LED.

# 1.10.6 FLASH-drive

CPC152 modules are equipped with Flash-memory microchip, using NAND (SLC) technology. It can be used as the boot drive, can be turned OFF in BIOS SETUP settings or by the jumper. For accessing to NAND Flash, IDE controller with integrated error correction and wear adjustment systems will be used, and it is connected to IDE interface of CPU (Primary Channel).



# Attention!

Volume of integrated drive in CPC152 – 2 GB (available volume – 1.8 GB).



# Attention!

In case of joint use of Compact Flash module and integrated FLASHdrive, as well as if only integrated FLASH-drive (without additional accessories connected to IDE ports) is used, it is recommended to set operation mode of the integrated FLASH-drive to "Primary Master" (using the group of jumpers X3 and X4, see Section <u>3.1.11 Purpose of integrated IDE devices</u>).

Compact Flash cards of 1/2 types and external devices with IDE interface can be used as additional drive memory.

Selection of operation mode of Compact Flash and soldered FLASH-drive (Primary Master / Slave) is carried out using jumpers.

Integrated Flash-drive is connected to IDE-controller, integrated into the CPU. In this case, its operation could require a standard IDE driver.

# 1.10.7 Compact Flash (XP1)

The Compact Flash (CF type I / II) device can be connected to the module via XP1 (N7E50-M516RB-50, 3M) and uses the same channel ("Primary") that is used with UIDE interface. In this case, if it is used, connection of only one IDE device is possible. Compact Flash device, as a storage, can be operated in "Master" / "Slave" modes, as well as it can be used as a boot drive.



# Attention!

USING THE MODULE UNDER SEVERE OPERATING CONDITIONS IT IS REQUIRED TO TAKE FURTHER MEASURES FOR FIXING THE COMPACT FLASH INTO THE CONNECTOR

Capacity of CompactFlash →	3003 AB	3004 AB	3005 //B	8006 B	8007 B	8008 B	8009 B	3010 iB	3011 iB	3012 iB
$\downarrow$ Configuration $\downarrow$	MIC23003 128MB	MIC23004 256MB	MIC23005 512MB	MIC23006 1GB	MIC23007 2GB	MIC23008 4GB	MIC23009 8GB	MIC23010 16GB	MIC23011 32GB	MIC23012 64GB
NAND – master CF – slave	+	+	+	+	+	+	+	+	+	+
NAND – slave CF – master	+	+	+	+	+	+	+	+	+	+
Only CF – master	+	+	+	+	+	+	+	+	+	+
Only CF – slave	+	+	+	+	+	+	+	+	+	+
HDD - master CF – slave	-	-	-	_	-	-	_	_	-	-
HDD – slave CF – master	-	-	-	_	+	+	+	+	+	+
CD/DVD – slave CF – master	-	-	-	_	-	_	_	-	-	_
CD/DVD – master CF – slave	+	+	+	+	+	+	+	+	+	+

Table 1-2. Table of available combinations of IDE devices with MIC230X	Table 1-2:	Table of available combinations of IDE devices with MIC230xx
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# 1.10.8 IDE port (XP16)

Two "HDDs" with IDE interface can be connected to the module via KIB98201 interface board (connector XP16 of CPC152) and use the "Primary" channel for operation in "Master" / "Slave" modes.

In case of using two external devices, the Compact Flash should be preliminary disconnected from XP1 connector, and the integrated FLASH-drive is disconnected using the respective jumpers – see section Setting module's switches. IDE interface supports UDMA/100 mode (cable length during connection should not exceed 0,1 m).

2,5" HDD devices are connected to J2 of KIB98201 interface board (not included into the delivery checklist, to be purchased separately) using the ACS00010 cable (not included into the delivery checklist, to be purchased separately). Other HDD types (3,5") and CD/DVD write and read devices, having 40-pin connector (with a pitch of 2,5 mm), are connected to the module, to J1 of KIB98201 interface board, using the standard IDE cable.

Using other types of cables, it is recommended for connection to use cables with connectors of 2040-3442 (Leotronics) or IDC2-44 types (socket 44 pins for the ribbon, with a pitch of 1 mm).



# Attention!

When connecting Compact Flash modules to IDE port using IDE– Compact Flash adapters, it is permissible to use only Compact Flash modules, supporting UDMA-5 and higher modes (e.g. MIC230 modules with a volume from 2 GB and more).

Using other Compact Flash cards could result in damage of CPC152 module (damage of integrated FLASH-drive) and would not be

considered as warranty case (caused by various voltage levels on signal IDE lines for various Compact Flash modules).

For Compact Flash modules, installed into XP1 connector (located on CPC152 module) there are no such limitations.



# Attention!

When connecting such external devices as HDDs or CD/DVD reading device to IDE port with the use of KIB98201 interface board, it is permitted to use a cable with a length not exceeding 140 mm (ACS00016-01 or ACS00016-02), available IDE cable length from KIB98201 to an external device – no more than 100 mm.

When connecting two external devices, it is allowed to use a standard IDE cable (in this case the FLASH-drive should be turned OFF, and Compact Flash module should be removed from the XP1 connector).

Available combinations for the connection of internal and external IDE devices are specified in the table below.

	FLASH-drive Slave	Compact Flash Slave	HDD Slave	CD/DVD Drive Slave
FLASH-drive Master		+	+	-
Compact Flash Master	+		-	-
HDD Master	-	+		+
CD/DVD Drive Master	+	+	+	

Table 1-3:	Table of allowable combinations of IDE devices
------------	--

# 1.10.9 GPIO port (XP10)

GPIO port is implemented on the basis of GPIO\_P2[7:0] port of Vortex86DX CPU. Port lines are tolerant to the voltage level 5V. Each port line can be configured as input or output

Modes of using the GPIO port:

- Digital I/O port
- Control of servo drives (PWM signal)
- Mode of compatibility with 8051

In order to ensure the certainty of state of GPIO port lines, after power is ON it is recommended to use a dedicated line of power supply voltage (+5VEXT, output #9 of XP10 connector) for feeding the logical circuitry, connected to the GPIO port, as well as using a binding to high (+5V) or ground (GND) levels immediately in the devices connected to the port. When connecting external devices, common wire (connector XP10, output 10) connection is obligatory.

GPIO port is routed to the XP10 connector (98424-G52-10LF, FCI).

For manufacturing cable for GPIO port, it is recommended to use the 10-pin socket for ribbon cable with a pitch of 1 mm: 89947-710LF (FCI).

Fig. 1-4: Numbering of XP10 connector contacts



# 1.10.10 Serial ports COM1/ 2/ 3/ 4 (XP3, XP4, XP6, XP7)

CPC152 has 4 asynchronous serial ports

- COM1 (XP3 connector), COM2 (XP4 connector) RS-422/485 (4- / 2-wire power on)
- COM3 (XP6 connector), COM4 (XP7 connector) RS-232 (full 9-wire interface).

Exchange rate via serial ports can be set in the BIOS Setup settings. Exchange rate is defined by the value of CPU frequency divider register. Divider's value is calculated by the formula:

 $DIV = F / (16 \cdot BR), BR = F / (DIV \cdot 16)$ 

- F frequency of internal generator [MHz] (1.8432 or 24);
- DIV divider's value (for F = 1.8432 MHz minimum value DIV = 1; for F = 24 MHz - minimum value DIV = 2);
- BR required speed of exchange, [bit/sec].



# Attention!

The receiver tolerates deviation of the exchange speed value by 3.0% to the lesser side and by 2.5% to the greater side

The table below contains frequency divider's values for a number of exchange speeds using an internal generator: 8432 MHz and 24 MHz:

Exchange speed,	F=1.84	132 MHz	F=24 MHz			
bit/sec	Divider	Error, %	Divider	Error, %		
50 2304		0.000	30000	0.000		
75	1536	0.000	20000	+0.002		
110	1047	-0.026	13636	0.000		
150	768	0.000	10000	0.000		
300	384	0.000	5000	0.000		
600	192	0.000	2500	0.000		
1,200	96	0.000	1250	0.000		
1,800	64	0.000	833	+0.040		
2,000	58	+0.69	750	0.000		
2,400	48	0.00	625	0.000		
3,600	32	0.00	417	-0.079		
4,800	24	0.00	312	+0.160		
7,200	16	0.00	208	+0.160		
9,600	12	0.00	156	+0.160		
19,200	6	0.00	78	+0.160		
38,400	3	0.00	39	+0.160		
57,600	2	0.00	26	+0.160		
115,200	1	0.00	13	+0.160		
250,000	_	-	6	0.000		
256,000	_	-	6	-2.340		
375,000	_	_	4	0.000		
500,000	_	_	3	0.000		
750,000	_	_	2	0.000		

#### Table 1-4: Frequency divider values for serial ports

**CPC152** 

# 1.10.10.1 COM1 / COM2 (RS-422/485)

COM1 and COM2 ports operate in the RS-422/485 mode and ensure galvanic isolation of up to 500 V (each port is equipped with individual isolation from the system). Maximum data exchange speed – 115 2000 bit/sec. The ports are routed to one row WAGO 733-335 connectors with 5 outputs.

As transmitter-receivers, integral solutions based on LTM2881IV-5 (Linear Technology).are used

Through installation of X10 jumpers ... X14 (COM1), X15 ... X19 (COM2) consistent circuits will be connected to signaling lines of RS-422 or RS-485 interfaces and operation mode will be set.



# Attention!

For proper operation of transmitter-receivers RS-422/485, in multiterminal networks it is required to install line terminators for 120 Ohm using relevant jumpers at two the most remote network nodes, as well as biasing resistors for 680 Ohm (on one or two of the most remote network nodes).

Depending on the default configuration, each port contains lightning protection circuits, based on self-recovering fuses and gas discharge elements. The port also contains protection circuits against pulse interference on the basis of TVS-diodes. Diagram of output stages of COM1 port is specified below (COM2 port has a similar circuit design).









Fig. 1-7:

Connection of modules via RS-422 interface



For manufacturing the cable it is required to use a removable part of WAGO 733-105 terminal block and shielded twisted pair.

#### Fig. 1-8: Numbering of contacts of XP3, XP4 connectors



# 1.10.10.2 COM3 / COM4 (RS-232)

COM3 and COM4 ports operate in the full 9-wire mode of RS-232 interface and have standard basic addresses for PC/AT. Integral solutions based on ADM3311EARU (Analog Devices) are used as transceivers.

The both ports can be used for console input/output and loading of files. For connection with PC, used as hyperterminal, the null-modem cable is required. *COM3 port is used by default.* 

Maximum speed of data transfer for COM3 and COM4 is 115.2 Kb/sec. The ports are fully software compatible with UART 16550 version.

COM3 and COM4 ports are routed to XP6 and XP7 connectors respectively, IDC10 2.54mm (5104338-1, AMP).

For connection to COM3 and COM4 ports, ACS00005-01 cable (1 pcs. included into the delivery checklist) is used.

For proprietary manufactured cable it is recommended to use 10-pin socket for the ribbon cable with a pitch of 1.27 mm: 1-215919-0 (AMP).

Fig. 1-9: Numbering of contacts of XP6 and XP7 connectors

# 1.10.11 PS/2 keyboard and mouse pointing device (XP8)

Interface for the connection of PS/2-keyboard and mouse is routed to the 6-pin XP8 connector.

PS/2 keyboard or mouse can be connected via ACS00043 adapter cable. For proprietary manufacturing of the adapter cable it is recommended to use PHR-6 (JST) socket with contacts SPH-002T-P0.5S (JST). For connection of both keyboard and mouse, it is required to additionally use a standard Y-cable.

Fig. 1-10: Numbering of XP8 connector contacts

Additional PS/2 keyboard or mouse can be connected to the standard MiniDIN-6F, located on the KIB98201 interface board (J4). For connection of both keyboard and mouse, it is required to additionally use a standard Y-cable.

# 1.10.12 USB ports (XS1, XP21)

The module has 4 USB Host ports with support of USB 1.1 and USB 2.0 specifications.

In terms of design, the USB ports represent a dual XS1 connector of USB-A type, installed on the brink of module's board and a vertical two row 10-pin XP21 connector of IDC2-10 type with a pitch of 2 mm (98424-G52-10LF, FCI). In this case, two channels USB0 / USB1 are routed to the standard XS1 connector, two others USB2 / USB3 – to XP21 connector.

Each pair of channels has an individual power scheme. Purpose of XP1 (USB-A) connector's contacts corresponds to the one set by USB specification. Purpose of XP21 (IDC2-10) connector's contacts is specified in the relevant table.

Connection of USB devices to USB2/USB3 ports is available through the adapter cable ACS00051. For proprietary manufacturing of the cable for USB2 / USB3 ports it is recommended to use 10-pin socket to the ribbon cable with a pitch of 1 mm - 89947-710LF (FCI).





#### 1.10.13 LAN 10/100 Mb port (XS2)

The module has one LAN port with the exchange speed of -10 / 100 Mb/sec and is implemented on the basis of LAN 10/100 Mb controller integrated into the CPU.

LAN channel is routed to the standard XS2 connector of RJ-45 type, installed on the verge of module's board. Purpose of connector's contacts corresponds to the one set by the standard IEEE 802.3 Ethernet specification.

# 1.10.14 LPT parallel port (XP5)

Universal parallel port with support of SPP (PC-compatible printer port), EPP (Extended Capabilities Port), ECP (Enhanced Parallel Port) modes. The interface is routed to the connector of IDC type, pitch of 2.54 mm, 26 pins (5104338-6, AMP).

For cable manufacturing it is recommended to use the 26-pin socket to the ribbon cable with a pitch of 1.27 mm – 2-215919-6, AMP.

_	2												26	
	0	0	0	0	0	0	0	0	0	0	0	0	0	
	0	0	0	0	0	°	0	2	0	0	0	0	0	
<u> </u>	1												25	_

In addition, LPT port is routed to the XP16 for the connection of LPT devices to the DSUB-25F connector (J5) on KIB98201 interface board.

# 1.10.15 RTC, SPI FRAM, lithium battery

CPC152 module is equipped with AT-compatible real-time clock with the lithium battery installed (XS7 socket).

The expected (standardized) operating time of the battery at turned-off or lacking integrated circuit of non-volatile RAM of 128 KB - approx. 10 years<sup>7</sup>. However, the service life of the battery depends on operating temperature as well as on the length of the period within which the system is off.

 $<sup>^{7}</sup>$  Under normal conditions (humidity from 5 to 95%, +25°C).



#### Important note:

It is recommended to replace the battery in about 4 years of service, not waiting for the end of its service life.

#### Important note:

During battery replacement, polarity should be observed (+ above).

The used batteries should be utilized in accordance with the established standards.

FRAM nonvolatile memory with a serial SPI interface is designed for saving the SETUP BIOS copy and recovery of RTC memory state in case of an error, as well as for storing gauge coefficients of analog-to-digital converter/digital-to-analog converter. User has also access to free FRAM cells. Access is provided via INT 17H BIOS function. Memory volume available to the user amounts to 7 KB.

Switching to the main voltage of 3.3 V instead of battery voltage when the power supply is on, ensures additional resource economy of the installed lithium battery.

For use of CPC152 modules with conformal coating, there is a possibility of connecting an external battery. For this purpose, an additional XP22 connector (ACS00058, a set of Li battery of 3V with PHR-2 connector, length of 40 mm) is provided. For proprietary manufacturing of the cable it is recommended to use PHR-2 (JST) socket with SPH-002T-P0.5S (JST) contacts.



#### Important note:

If an external battery is connected to the additional XP22 connector, it is required to remove the Li batter from XS7 socket. During installation, polarity should be observed ("+" corresponds to the first contact of the connector).

Fig. 1-13: Numbering of XP22 connector contacts

	1	2	
ſ			
ŀ			

# 1.10.16 Port of isolated remote reset / interrupt (XP17, XP18)

When connecting to the XP18 contacts of an external button / potential-free contact, it is possible to generate an external reset or interrupt signal, isolated from the system (500 V).

In order to receive the reset signal using XP18 connector, it is required to close the contacts of XP18 / 1 and XP18 / 2 connectors, where XP18 / 2 is directly connected with GNDS1 circuit (common wire/ground of isolated RS-422/485 interface, COM1).

For receipt of reset signal, using XP17 connector, it is required to feed the voltage to contacts of XP17 / 1 and XP17 / 2 connectors, depending on the installed X23 jumper – 3...15 V or 10...30 V.

The reset / interrupt signal is generated via or from the sources, connected to XP17, XP18. Connectors are isolated from each other.

For manufacturing of the cable it is required to use the PHR-2 (JST) socket with SPH-002T-P0.5S (JST) contacts.

Fig. 1-14: Numbering of XP17, XP18 connectors contacts



# 1.10.17 PC/104 extension bus (ISA 8/16 bit)

PC/104 (XS4) connector is designed for installation of extension modules in PC/104 format to the module. It is possible to install no more than 4 PC/104 extension modules.

# Fig. 1-15: Numbering of contacts of XS4 connector a) top view of the module, b) bottom view of the module with personal organizer, installed on the connector



# 1.10.18 MicroPC extension bus (ISA 8 bit)

Edge connector MicroPC (XS6) is designed for installation of CPC152 into MicroPC mounting frame and for extension of system functionality by way of installing extension modules in MicroPC format into the frame. It is possible to install no more than 8 extension modules in MicroPC format.



# Attention!

Connection of FDDs in MicroPC format is not supported (however, connection of an external drive to the USB port).

# 1.10.19 Diagnostic LEDs

For indication of various conditions, the module is equipped with separately located LEDs, as well as 2 LEDs, integrated into the XS2 connector. The LEDs are installed from TOP side. Purpose of module's LEDs is specified in the table.

LED	Function
HL1	Two-color user LED (red / green)
HL2	Activity of IDE-devices (green)
HL3	Indication of module's hardware reset (green)
HL4	Indication of watchdog timer actuation (red)
HL5	Indication of module's power supply (green)
XS2 / HL6	LED of network interface controller activity (green)
XS2 / HL7	LED of network interface controller operation mode (yellow)

#### Table 1-5: Purpose of CPC152 LEDs

HL1 LED is controlled via recording to the integrated circuit register FPGA (input/output space, ISA bus).

# 1.10.20 JTAG port (XP9)

JTAG (XP9) connector is used during module production and represents a process connector.

# 1.10.21 Acceleration, pressure and temperature sensors

As acceleration sensor, a capacitance integrated sensor MMA8451Q (Freescale) is used. With resolution of 8/14 bit this sensor enables to measure acceleration via three axes, vibrations in ranges 2/4/8 g, determine a slope angle, free fall, ripples and shocks.

The module also includes a digital integrated pressure sensor MPL115A2 (Freescale), which enables to measure pressure in the range from 50 to 115 kPa (standard measurement accuracy amounts to 1 kPa in the operating temperature range from -20 to +85°C).

Additionally, the module is equipped with temperature sensor LM92CIM (National Semiconductor), which enables to measure temperature on module's surface with resolution of 12 bit (+ sign) in the range from -55 to +125°C. The sensor is located in the Vortex86DX CPU area.

Acceleration, pressure and temperature sensors are connected to I2C bus of the CPU. Measurement area is not rated, the standard error is defined by characteristics, stated by sensors manufacturer.

In order to use the sensors as measuring sensors it is required to perform their calibration testing (system of calibration factors storage maybe arranged on the basis of FRAM nonvolatile memory, which main principles of operation are specified in <u>Section 4.6 "Interface BIOS SOC Vortex86DX for read/write in FRAM"</u>).

# 1.10.22 Audio port

Audio port in CPC152 module is implemented on the basis of integrated circuit CMI8738MX (Cmedia), including a sound controller and 16-bit audio codec.

Codec is compatible with SBPRO<sup>™</sup> version.

the set of audio ports includes: LINE-IN (Stereo), LINE-OUT (STEREO) and MIC (MONO).

Audio ports are routed to the XP15 connector. Connection of devices is possible via KIB98102 interface board, on which these interfaces are routed to the standard "Audio Jack" type connectors.


#### Attention!

For proper operation of Audio ports it is required to remove the jumpers XP1[1-2], XP2[1-2] and install jumpers XP3[1-2], XP4[2-3] on interface board KIB98102.

Use of KIB98101 is not recommended, since KIB98101 does not provide compatibility with a number of TFT-panels and does not ensure an accurate playback/record of sound.

#### 1.10.23 Video port (Analog RGB and TFT)

Video subsystem of CPC152 is implemented on the basis of SM718KE160000-AB video processor. Video controller with 2D accelerator function has the following technical characteristics and capacities:

- Volume of integrated video memory 16 MB DDR;
- Possibility of connecting LCD (TFT) panels with TFT interfaces and resolution of no more than 1920 x 1440 (60 Hz), color depth of no more than 18 bit;
- Possibility of connecting RGB (VGA) displays with resolution of no more than 1920 x 1440 (75 Hz, 32 bit).

TFT and Analog RGB ports are routed to the XP15 connector. Connection of devices is possible via KIB98102 interface board, on which these interfaces are routed to IDC-34 (TFT) and DSUB-15F (Analog RGB) connectors.

Using the X6 jumper on CPC152 makes it possible to select the power supply voltage of TFT-panel (+3.3 / +5 V).

An additional XP2 connector (98424-G52-10LF, FCI) is also provided for the connection of display or TFT-panel to the Analog RGB port by a separate cable to XP2 connector without the use of KIB98102 interface board. For the connection, ACS00027-02 cable will be required (not included into the Delivery Checklist, to be purchased as an option).

For proprietary manufacturing of the cable it is recommended to use the 10 pin socket to the ribbon cable with a pitch of 1 mm - 89947-710LF (FCI).

Numbering of XP2 connector contacts



#### 1.10.24 XP15, XP16 extension ports

For connection of such devices as TFT-panel, VGA-display, PS/2 mouse and keyboard in CPC152 module, an extension in the shape of XP15 connector (5-104068-6, AMP) is provided. This extension is designed for connection to CPC152 module of KIB98102 interface board. Connection to KIB98102 is carried out by cables ACS00015 (300 mm), ACS00015-02 (120 mm), ACS00015-03 (140 mm) or ACS00015-02 (500 mm).

For proprietary manufacturing of the cable for connection to the KIB98102 interface board it is recommended to use a 60-pin socket 1-111196-2 (AMP) with a pitch of 1.27 mm and a ribbon cable 57013-3 (AMP).

Fig. 1-16: External view of XP15 connector



#### Attention!

It is not recommended to use KIB98101 interface board jointly with the CPC152 CPU Module.

While connecting KIB9810<u>1</u> interface board instead of KIB9810<u>2</u> to CPC152, there are the following limitations:

- Power supply of the TFT-panel is possible only by a +5 V level (it is required to choose +5V power supply voltage using the X6 jumper), proper operation of TFT-panel in this case is not guaranteed;
- Limited functionality of Audio port (lack of electret microphones support, additional noises in LINE\_IN, LINE\_OUT channels).

For the connection of such devices as HDD 2.5", HDD 3.5", LPT in CPC152 module, an extension in the form of XP16 connector is provided. This extension is designed for the connection of KIB98201 interface board.

Connection to KIB98102 is carried out by cables ACS00016 (300 mm), ACS00016-02 (120 mm), ACS00016-03 (140 mm) or ACS00016-02 (500 mm).

For proprietary manufacturing of the cable for connection to the KIB98201 interface board it is recommended to use a 72-pin socket 1-111196-4 (AMP) with a pitch of 1.27 mm and a ribbon cable 1-57013-2 (AMP).



# **SECTION 2**

# **TECHNICAL INFORMATION**

# 2 TECHNICAL INFORMATION

## 2.1 General technical specifications of CPC152

#### Table 2-1: Requirements for power supply of CPC152

Requirements for power supply		
Power supply voltage	+5 V $\pm$ 5%; 12 V <sup>8</sup>	
Module current consumption over +5 V (without external device	es, at +25°C), no more than:	
CPC152-01	0.85 A	
Maximum available consumption current over external circuits, temperature range (is limited by the installed short-circuit prote		
+5V_EXTU1 (XS1: port USB1, +5V)	500 mA @ +5 V	
+5V_EXTU2 (XS1: port USB2, +5V)	500 mA @ +5 V	
+5V_EXTP (XP5: LPT port)	500 mA @ +5 V	
+5V_EXTR (XP6, XP7: COM3/COM4 ports)	500 mA @ +5 V	
+5V_EXTK (XP8: PS/2 keyboard/mouse port)	500 mA @ +5 V	
+5V_EXTM (XP15: connection to KIB98102, PS/2 port)	500 mA @ +5 V	
VCC_EXTF (XP15: connection to KIB98102, TFT port)	500 mA @ +3.3/+5 V	
+5V_EXTD (XP15: connection to KIB98201)	1500 mA @ +5 V	
+5V_EXTL (XP14: PC-buzzer port; XP10: GPIO port)	500 mA @ +5 V	
+5V_EXTU3 (XP21: port USB3, +5V)	500 mA @ +5 V	
+5V_EXTU4 (XP21: port USB4, +5V)	500 mA @ +5 V	
Maximum available total consumed current (with due consideration of internal and external circuits)	5.5 A	

#### Table 2-2: Characteristics of digital inputs-outputs (GPIO)

Digital inputs-outputs	
Input voltage Log. "0"	max. 0.8 V
Input voltage Log. "1"	min. 2.0 V
Output voltage Log. "0" (at a current of 5 mA)	max. 0.4 V
Output voltage Log. "1" (at a current of 2 mA)	min. 2.4 V
Load-carrying capacity of Log."0"/ Log."1" (TTL-levels)	16.0 / 4.0 mA

<sup>&</sup>lt;sup>8</sup> Required only for illumination of LCD panels

Serial ports	
Maximum exchange speed over RS-232	250 Kb/sec <sup>9</sup>
Maximum exchange speed over RS-422/485	750 Kb/sec
Voltage of RS-422/485 ports isolation from the system	500V
ESD protection	15 kW (IEC1000-4-2)

#### Table 2-3: **Characteristics of serial ports**

#### Table 2-4: Characteristics of USB, LAN ports

USB, LAN ports	
Type of USB ports	USB Host
Type of supported USB devices	1.1, 2.0
Exchange speed over LAN port	10 / 100 Mb/sec
LED activity indication of LAN channel	green LED – activity, yellow LED – operation mode (full - / half-duplex)
LAN port isolation	500V

#### Table 2-5: **IDE** port characteristics

IDE port	
Volume of integrated FLASH-drive	1 GB
Supported types of Compact Flash cards	1/2
Supported IDE-device operation modes	up to Ultra-DMA 100 <sup>10</sup>
Number of IDE devices	up to 2 devices

Table 2-6: Characteristics of integrated temperature, pressure, acceleration sensors

Temperature sensor		
Temperature measurement range	-55+125°C (complementary code with a sign)	
Type of sensor used	LM92CIM (National Semiconductor)	
Rated absolute temperature measurement error <sup>11</sup>	± 0.5°C (+10+50°C) ± 1.0°C (-10+85°C) ± 2.0°C (-40+85°C)	
Resolution	12 bit + sign	
Price of the least significant digit value	0.0625°C	
Conversion time	up to 1000 ms	

<sup>&</sup>lt;sup>9</sup> Exchange speed over serial ports is defined by the value of frequency divider register, in the BIOS Setup settings, maximum standard frequency – 115200 Kb/sec. <sup>10</sup> Setting of UltraDMA-5 mode is only possible if the integrated drive is solely active and this drive is set as Primary Master,

and other devices are not connected to IDE interface.

relative error is not rated, data specified in the table are guaranteed by sensor manufacturer and are not verified during the tests

Pressure sensor		
Measurement range	50115 kPa	
Type of sensor used	MPL115A2 (Freescale)	
Rated absolute pressure measurement error	± 1.0 kPa (-20+85°C)	
Resolution	10 bit	
Price of the least significant digit value	0.15 kPa	
Conversion time	up to 3 ms	
Acceleration sensor		
Measurement ranges	± 2g / ± 4g / ± 8g (additional code with a sign)	
Type of sensor used	MMA8451Q (Freescale)	
Resolution	14 bit + sign	

Table	2-7:	Environmental conditions
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Environmental conditions	
Operating temperature range	-40+85 °C
Storage temperature	Modules storage conditions 1 in accordance with GOST 15150-69
Humidity	up to 95% at +25 °C without condensation

#### Table 2-8: Mechanical characteristics

Mechanical characteristics	
Vibration resistance	5 g (acceleration amplitude)
Resistance to single shocks	100 g (peak acceleration)
Resistance to multiple shocks	50 g (peak acceleration)
Dimensions, no more than	$125.0 \times 123.0 \times 27.0 \text{ mm}$
Weight, no more than	140 g
MTBF, no less than <sup>12</sup>	160 000 hours

<sup>&</sup>lt;sup>12</sup> MTBF values are calculated using the Telcordia Issue 1 computation model (Method I Case 3 calculation technique) for continuous operation in case of the ground-based placement under the conditions, corresponding to the climatic category "Moderately Cold Climate 4" according to the GOST 15150-69, at ambient temperature of + 30°C.

## 2.2 Allocation of hardware interrupts

#	Default source	Alternative sources
NMI	-	<ul> <li>Internal WDT</li> <li>SYSTEM EVENT *</li> <li>External ISA – devices (IOCHCK#)</li> </ul>
IRQ0	Reserved (system timer)	-
IRQ1	PS/2 Keyboard	-
IRQ2	Reserved (cascading)	-
IRQ3	COM2 (RS-422/485) / COM4 (RS-232)	<ul> <li>External ISA – devices (IRQ3)</li> </ul>
IRQ4	COM2 (RS-422/485) / COM3 (RS-232)	<ul> <li>External ISA – devices (IRQ4)</li> </ul>
IRQ5	LPT port	<ul> <li>USB controller</li> <li>External ISA – devices (IRQ5)</li> </ul>
IRQ6	USB controller*	<ul><li>External ISA – devices</li><li>Internal WDT</li></ul>
IRQ7	– (see <u>Registers of control / interrupts condition</u> )	<ul> <li>External ISA – devices (IRQ7)</li> <li>SYSTEM EVENT ***</li> <li>Internal WDT</li> </ul>
IRQ8	RTC (Real Time Clock )	-
IRQ9	External ISA – devices (IRQ9)	-
IRQ10	External ISA – devices (IRQ10)	_
IRQ11	<ul> <li>(see <u>Registers of control / interrupts condition</u>)</li> </ul>	<ul> <li>External ISA – devices (IRQ11)</li> </ul>
IRQ12	PS/2 Mouse**	<ul> <li>USB controller</li> <li>External ISA – devices (IRQ12)</li> </ul>
IRQ13	Reserved (support of coprocessor)	-
IRQ14	Primary IDE (HDD, Compact Flash,)	<ul> <li>External ISA – devices (IRQ14)</li> </ul>
IRQ15	LAN controller	<ul> <li>SYSTEM EVENT ***</li> <li>External ISA – devices (IRQ15)</li> </ul>

 Table 2-9:
 Addresses of hardware interrupts

\* USB controller by default occupies IRQ6 interrupt line. If the LPT port is switched off in the BIOS Setup settings, the USB controller occupies IRQ5 line.

\*\* Use of alternative sources is possible only when switching off the PS/2 Mouse support in BIOS Setup settings (see "Boot -> Boot Settings Configuration", parameter "PS/2 Mouse Support").

\*\*\* The following sources are combined over "or" inside the FPGA and can be switched to the input of relevant interrupt by way of recording to the respective FPGA control register (hereinafter referred to as the "SYSTEM EVENT").

- PFO (power supply +5V reduction lower than the level of 4.65 V)
- External WDT
- External optoisolated input

## 2.3 Channels of DMA module

Table 2-10: Channels of DMA module

#	Source
DRQ0	-
DRQ1	LPT/ External ISA – devices
DRQ2	External ISA – devices
DRQ3	External ISA – devices
DRQ5	External ISA – devices
DRQ6	External ISA – devices
DRQ7	External ISA – devices

## 2.4 I/O address space

Table 2-11:	Allocation of the I/O address space
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Address	Function	Notes		
0000h – 001Fh	8237 DMA Controller #1	_		
0020h – 0021h	8259 Master Interrupt Controller	-		
0022h – 0023h	Indirect Access	WDT0		
0024h – 002Dh	ISA bus	Access to external bus		
002Eh – 002Fh	Reserved	Not available		
0030h – 003Fh	ISA bus	Access to external bus		
0040h – 0043h	8253 Programmable Timer	-		
0044h – 0047h	ISA bus	Access to external bus		
0048h – 004Bh	Reserved	Not available		
004Eh – 005Fh	ISA bus	Access to external bus		
0060h – 0064h	8042 Keyboard Controller	_		
0065h	WDT0	-		
0066h	ISA bus	Access to external bus		
0067h – 006Dh	WDT1	-		
006Eh – 006Fh	ISA bus	Access to external bus		
0070h – 007Fh	RTC, NMI Mask Register	-		
0080h – 009Fh	DMA Page Registers	-		
00A0h – 00B1h	8259 Slave Interrupt Controller	_		
00B2h – 00BFh	ISA bus	Access to external bus		
00C0h – 00DFh	8237 DMA Controller #2	_		
00E0h – 01EFh	ISA bus	Access to external bus		

Address	Function	Notes
01F0h – 01F8h	Primary IDE Controller	_
01F9h – 0277h	ISA bus	Access to external bus
0278h – 027Fh	LPT port	(possible value)
0280h – 028Fh	Internal control registers	I/O ports of matrix keyboard, LEDs, analog I/O, internal control registers (PLD XCS05)
0290h – 029Fh 02A0h – 02AFh 02B0h – 02BFh	-	-
02C0h – 02E7h	ISA bus	Access to external bus
02E8h – 02EFh	COM2	(possible value)
02F0h – 02F7h	ISA bus	Access to external bus
02F8h – 02FFh	COM4	(possible value)
0300h – 0377h	ISA bus	Access to external bus
0378h – 037Fh	LPT port	(possible value)
0380h – 03AFh	ISA bus	Access to external bus
03B0h – 03BBh	MDA Adapter	(possible value)
03BCh – 03BFh	LPT port	(possible value)
03C0h – 03CFh	EGA, VGA Adapter	(possible value)
03D0h – 03DFh	CGA Adapter	(possible value)
03E0h – 03E7h	ISA bus	Access to external bus
03E8h – 03EFh	COM1	(possible value)
03F0h – 03F7h	Floppy Controller #1	(possible value)
03F8h – 03FFh	СОМЗ	(possible value)
0400h – 04CFh	ISA bus	Access to external bus
04D0h – 04D1h	Reserved	Not available
04D2h – 0777h	ISA bus	Access to external bus
0778h – 077Fh	Reserved	Not available
0780h – 0CF7h	ISA bus	Access to external bus
0CF8h – 0CFFh	Configuration registers of host PCI controller	-
0D00h – EDFFh	ISA bus	Access to external bus
EE00h – EF3Fh	Reserved	Not available
EF40h – FBFFh	ISA bus	Access to external bus
FC00h – FC0Dh	Reserved	Not available
FC0Eh – FFEFh	ISA bus	Access to external bus
FFF0h – FFFFh	Reserved	Not available

Address	Port	Notes
BA+00h	BA*	Setting a base address of internal PLD registers (BA=0280h by default)
BA+01h	Port of LEDs control	Program control of LEDs
BA+02h BA+03h	-	
BA+04h	-	
BA+05h	Port of control of NMI / IRQ interrupt sources	Port of interrupts control over NMI / IRQ line of CPU (External WDT, Power Fail, SYSTEM EVENT, ISA\$IOCHK#)
BA+06h BA+07h	Port of control of IRQ7,11,12,15 interrupt sources Port of ISA control	Port of IRQ7,11,12,15 interrupts control of CPU (sets the source over interrupt lines of CPU: ISA\$IRQx, SYSTEM EVENT). Activation / Deactivation of ISA bus buffers.
BA+08h – BA+0Bh	-	
BA+0Ch BA+0Dh	-	
BA+0Eh	Number of PLD XCS05 firmware version	Codes from "00" to "255"
BA+0Fh	-	

#### Table 2-12: Internal I/O addresses

\* see register description "Port of base address (BA) control".

Table 2-13:         Memory devices addresses								
Address	Device	Notes						
00000 – 9FFFFh	DOS	DOS Area 640 Kbyte						
A0000 – BFFFFh	VGA	Video memory space 128 Kbyte						
C0000 – C7FFFh	VGA BIOS	VGA BIOS 32 Kbyte						
D8000 – DFFFFh	NV SRAM *	Non-volatile RAM 128Kbyte (page access, 16 KB)						
E0000 – EFFFFh	System BIOS	Extended System BIOS area 64 KB (16 KB x 4)						
F0000 – FFFFFh	System BIOS	System BIOS area 64 KB						

## 2.5 Memory address space

Address	Device	Notes
10 0000 - MEMORY TOP **	DRAM	DDR2 SDRAM
MEMORY TOP ** - FFE0 0000	PCI	PCI
FFE0 0000 – FFFF FFFFh	High BIOS	High BIOS Area 2 Mbytes (mapped to PCI)

\* Number of current page of non-volatile RAM is software selectable via I/O port (BA+0x0C).

\*\* Volume of installed memory DDR2 SDRAM - 256 Mbyte.

## 2.6 Use of GPIO ports of CPU

Vortex86DX microchip is equipped with 4x I/O GPIO (General Purpose Input Output) ports, available for the user via internal microchip registers. Each port represents 8x I/O lines, each of these lines can be set as an input or output by programming the registers of the relevant port.

For operation with GPIO ports, by two 8-bit registers per port will be used – date register and direction register. Each data register bit is matched with the relevant circuit on the board: Bit 0 corresponds to the line of 0 port (GPIO\_Px0), bit 7 corresponds to the line of 7 port (GPIO\_Px7) etc. Each bit of the direction register is matched with the respective circuit on the board. Bit 0 corresponds to the line of 0 port (GPIO\_Px0), bit 7 corresponds to the line of 7 port (GPIO\_Px7) etc.

	GPIO_P0	GPIO_P1	GPIO_P2	GPIO_P3	Description
Data register	78h	79h	7Ah	7Bh	
Direction register	98h	99h	9Ah	9Bh	0: Line is an input 1: Line is an output

Table	2-14:	GPIO control registers
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Purpose of the used GPIO ports is specified in the table below.

Line of I/O port	Direction of I/O line	Description
GPIO_P0[2:0]	input / output	Reserved. Lines used for configuring PLD.
GPIO_P0[3]	input	Interrupt input from temperature and accelerometer sensor. Active level: 1.
GPIO_P0[4]	input	Reserved. Lines used for configuring PLD.
GPIO_P0[5]	input / output	deactivation of video processor, switching to power saving mode.
GPIO_P0[6]	input	Reserved. Lines used for configuring PLD.
GPIO_P0[7]	input / output	Reset of external watchdog timer (changing the output state to the contrary restarts the WDT2 watchdog timer).
GPIO_P1[0]	input	Activation flag of WDT2 external watchdog timer: 0 – actuation was performed (booting from backup BIOS copy), 1 – actuation was not performed (booting from the main BIOS copy),
GPIO_P1[1]	input / output	Reserved (logics of switching to backup BIOS copy).
GPIO_P1[2]	input	Actuation of protection of USB ports power supply. 0 – actuation was performed, 1 – actuation was not performed,
GPIO_P1[3]	input	Error / malfunction in operation of one of the RS-422/485 transceivers (COM1/COM2). 0 – there was no malfunction, 1 – there was a malfunction.
GPIO_P1[4]	output	Connection of 120 Ohm terminator to A/B lines of COM1 port (RS- 422/485) 0 – 120 Ohm terminator is not connected, 1 – 120 Ohm terminator is not connected.
GPIO_P1[5]	output	Connection of 120 Ohm terminator to A/B lines of COM2 port (RS- 422/485) 0 – 120 Ohm terminator is not connected, 1 – 120 Ohm terminator is not connected.
GPIO_P1[6]	input / output	<ul> <li>When setting the GPIO_P16 port to the output - permit of operation of WDT2 watchdog timer, integrated into the power supply supervisor.</li> <li>0 – WDT2 watchdog timer is prohibited,</li> <li>1 – WDT2 watchdog timer is permitted.</li> </ul>
GPIO_P1[7]	input	Control of the integrated FLASH-drive. 0 – is deactivated 1 – is activated Line control only via BIOS Setup. GPIO line control only via CPU registers is not permitted!
GPIO_P2[7:0]	input / output	GPOI port, lines are routed to the XP10 connector. The lines are configured as "input" by default.
GPIO_P3[3:0]	-	Reserved (SPI FRAM interface).
GPIO_P3[5:4]	-	Reserved (I <sup>2</sup> C interface).
GPIO_P3[6]	input	Lithium battery condition: 3 V: 0 – battery needs to be replaced, 1 – battery is in proper operating condition.
GPIO_P3[7]	input / output	Reset of trigger condition of WDT2 watchdog timer, module restart. The line is configured as "input" by default.

Table	2-15:	Purpose of GPIO ports
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## 2.7 WDT0, WDT1 watchdog timers

Microchip of the Vortex86DX CPU is equipped with two adjustable hardware watchdog timers.

Access to registers of WDT0 timer is carried out via 65h port and 22h ports (Index address register) and 23h (Data register). For accessing registers, it is required to write the port address to the 22h port, which data reading and/or writing is carried out via 23h port. Tables 2-20...2-28 contain detailed description of control registers of WDT0 watchdog timer.

Access to the registers of WDT1 timer is carried out via 67h – 6Dh ports. The tables below 2-29...2-35 contain detailed description of control registers of WDT1 watchdog timer.

Address	Action									
Address	Action	7	6	5	4	3	2	1	0	
65h	Writing	RST_WDT0								
65h	Reading	-								

Table 2-16 WDT0 restart register

Any writing to this port will lead to the restart of WDT0 timer.

#### Table 2-17 Index register of WDT0 address port

Address	Action	Bits								
Address	Action	7	6	5	4	3	2	1	0	
22h	Writing	ADDR_REG_WDT0								
22h	Reading	-								

ADDR\_REG\_WDT0. Indicates address of the selected register of WDT0 watchdog timer for accessing via 23h data register.

#### Table 2-18 Data register of WDT0 port

Address	Action	Bits								
		7	6	5	4	3	2	1	0	
23h	Writing	WRDATA_REG_WDT0								
2511	Reading			WRDATA_REG_WDT0						

WRDATA\_REG\_WDT0. Contains data for writing to the internal register of WDT0 timer, which address is specified in the ADDR\_REG\_WDT0 field of 22h index register address.

WRDATA\_REG\_WDT0. Contains data when reading from the internal register of WDT0 timer, which address is specified in the ADDR\_REG\_WDT0 field of 22h index register address.

Table 2-19 Control register of WDT0 time
--

Address (in 22h address register)	Action	Bits (in 23h data register)								
		7	6	5	4	3	2	1	0	
37h	Writing	-	WDT0_WE	-	-	-	-	-	-	
(40h)	Reading	-	WDT0_WE	-	-	-	-	-	-	

## WDT0\_WE. Permission of WDT0 watchdog timer operation.

1 – permitted (default value);

0 - prohibited.

Tablo	2-20	Register of WDT0 event selection
rable	2-20	Register of wDTU event selection

Address (in 22h address register)	Action	Bits (in 23h data register)								
		7	6	5	4	3	2	1	0	
38h	Writing		WDT0	SSEL						
(D0h)	Reading									

WDT0\_SSEL. Selection of the event upon completion of WDT0 timer count.

0000 – reserved;
0001 – IRQ[3];
0010 – IRQ[4];
0011 – IRQ[5];
0100 – IRQ[6];
0101 – IRQ[7];
0110 – IRQ[9];
0111 – IRQ[10];
1000 – IRQ[11];
1001 – IRQ[12];
1010 – IRQ[14];
1011 – IRQ[15];
1100 – NMI;
1101 – module restart (default value);
1110 – reserved;
1111 – reserved.

Address (in 22h address register)	Action	Bits (in 23h data register)									
		7	6	5	4	3	2	1	0		
39h (00h)	Writing	WDT0_CNT0									
	Reading				WDT0_	_CNT0					

#### Table 2-21 CNT0 register of WDT0 timer value

# WDT0\_CNT0. Bits [7:0] of WDT0\_CNT counter [23:0] of WDT0 timer. The counter has a resolution of 30.5 µs

#### Table 2-22 CNT1 register of WDT0 timer value

Address (in 22h address register)	Action	Bits (in 23h data register)									
		7	6	5	4	3	2	1	0		
3Ah	Writing		WDT0_CNT1								
(00h)	Reading				WDT0	_CNT1					

WDT0\_CNT1. Bits [15:8] of WDT0\_CNT counter [23:0] of WDT0 timer. The counter has a resolution of 30.5 µs

Table	2-23	CNT2 register of WDT0 timer value	
Table	2-23	CNT2 register of WDT0 timer value	

Address		Bits (in 23h data register)								
(in 22h address register)	Action	7	6	5	4	3	2	1	0	
3Bh	Writing				WDT0_	CNT2				
(20h)	Reading	eading WDT0_CNT2								

WDT0\_CNT2. Bits [23:16] of WDT0\_CNT counter [23:0] of WDT0 timer. The counter has a resolution of 30.5 µs

Table	2-24	Register of WDT0 timer condition
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Address		Bits (in 23h data register)									
(in 22h address register)	s 7	6	5	4	3	2	1	0			
3Ch	Writing	WDT0_WDTF	WDT0_WDTRL	-	-	-	-	-	-		
(00h)	Reading	WDT0_WDTF	-	-	-	-	-	-	-		

WDT0\_WDTF. Flag of WDT0 timer actuation.

1 – there was a timer actuation (record "1" into this bit resets the flag);

0 – there was no timer actuation.

WDT0\_WDTRL. WDT0 timer restart.

1 – Reboot of WDT0\_CNT counter;

0 - This value is not allowed to be written.

#### Table 2-25 WDT1 restart register

Address	Action		Bits									
Address	Action	7	6	5	4	3	2	1	0			
67h	Writing	RST_WDT1										
67h	Reading	-	-	-	-	-	-	-	-			

Any writing to this port will lead to the restart of WDT1 timer.

Table	2-26	Control register of WDT1 timer	
1 4 5 1 0			

Address	Action				Bits				
Address	Action	7	6	5	4	3	2	1	0
68h	Writing	-	WDT1_WE	-	-	-	-	-	-
(00h)	Reading	-	WDT1_WE	-	-	-	-	-	-

WDT1\_WE. Permission of WDT1 watchdog timer operation.

1 – permitted;

0 - prohibited (default value);

Address	Action	Bits									
Address	Action	7	6	5	4	3	2	1	0		
69h	Writing		WDT1	SSEL		-	-	-	-		
(00h)	Reading	-	-	-	-	-	-	-	-		

WDT1\_SSEL. Selection of the event upon completion of WDT1 timer count. 0000 – reserved (default value);

0000 - reserved (defau
0001 – IRQ[3];
0010 – IRQ[4];
0011 – IRQ[5];
0100 – IRQ[6];
0101 – IRQ[7];
0110 – IRQ[9];
0111 – IRQ[10];
1000 – IRQ[11];
1001 – IRQ[12];
1010 – IRQ[14];
1011 – IRQ[15];
1100 – NMI;
1101 - module reboot;
1110 – reserved;
1111 – reserved.

#### Table 2-28 CNT0 register of WDT1 timer value

Address	Action				Bi	its					
Address	Action	7	6	5	4	3	2	1	0		
6Ah	Writing	WDT1_CNT0									
(00h)	Reading	WDT1_CNT0									

WDT1\_CNT0. Bits [7:0] of WDT1\_CNT counter [23:0] of WDT1 timer. The counter has a resolution of 30.5 µs

#### Table 2-29 CNT1 register of WDT1 timer value

Address	Action				Bi	ts				
Address	Action	7	6	5	4	3	2	1	0	
6Bh	Writing	WDT1_CNT1								
(00h)	Reading				WDT1_	_CNT1				

# WDT1\_CNT1. Bits [15:8] of WDT1\_CNT counter [23:0] of WDT1 timer. The counter has a resolution of 30.5 µs

#### Table 2-30 CNT2 register of WDT1 timer value

Address	Action				Bi	ts					
Address		7	6	5	4	3	2	1	0		
6Ch	Writing	WDT1_CNT2									
(00h)	Reading	WDT1_CNT2									

# WDT1\_CNT2. Bits [23:16] of WDT1\_CNT counter [23:0] of WDT1 timer. The counter has a resolution of 30.5 µs

Table 2-31 Register of WDT1 timer condition
---

Address	Action				Bits				
Address	Action	7	6	5	4	3	2	1	0
6Dh	Writing	WDT1_WDTF	-	-	-	-	-	-	-
(00h)	Reading	WDT1_WDTF	-	-	-	-	-	-	-

WDT1\_WDTF. Flag of WDT1 timer actuation.

1 – there was a timer actuation (record "1" into this bit resets the flag);

0 - there was no timer actuation.

## 2.8 Description of internal registers

### 2.8.1 Register of base address (BA) control

Used for setting the base address for module's internal registers.

Address	Action				Bi	ts			
Address	Action	7	6	5	4	3	2	1	0
BA+00h	Writing	-	-	BA9	BA8	BA7	BA6	-	-
BA+00h	Reading	0	0	BA9	BA8	BA7	BA6	0	0

BA[9:6] Enables to set the Base Address of module's internal control registers or address segment in I/O area, where these registers will be available for the system. If the address bits of ISA\_SA bus [9:6] match with the BA bits [9:6], internal registers will be addressed in read/write cycles in the I/O area.

BA value (after power on or hardware reset) by default = 0280h.

For example, in order to set *BA*=0300*h*, it is required to write 30*h* into the port. **Bit 5 and 4 of the base address (BA) always are written as equal to '0'.** 

### 2.8.2 Control / LED condition register

Enables a program control of two LED oscillators, as well as read their current condition.

Address	Action			Bits					
Autress	Action	7	6	5	4	3	2	1	0
BA+01h	Writing	-	-	-	-	-	-	LEDR	LEDG
BA+01h	Reading	-	-	-	-	-	-	SLEDR	SLEDG

 LEDG
 Green LED control.
 Write '1' - actuation of LED indicator, write '0' - deactivation.

 LEDR
 Red LED control.
 Write '1' - actuation of LED indicator, write '0' - deactivation.

 Clear
 Red LED control.
 Write '1' - actuation of LED indicator, write '0' - deactivation.

SLEDG <u>Green LED condition</u>. '1' - activated, '0' – deactivated (by default).

SLEDR <u>Red LED condition</u>. '1' - activated, '0' – deactivated (by default).

### 2.8.3 Interrupts condition register of ISA bus controller

Enables / prohibits to use external signals when generating an interrupt of NMI CPU, "SYSTEM EVENT" signal during writing to the port. The port also enables to determine a hardware source of NMI and "SYSTEM EVENT".

Address	Action	Bits								
Address	Action	7	6	5	4	3	2	1	0	
BA+02h	Writing	-	IRQ15_EN	IRQ12_EN	IRQ11_EN	IRQ10_EN	IRQ7_EN	IRQ4_EN	IRQ3_EN	
BA+02h	Reading	-	IRQ15_ST	IRQ12_ST	IRQ11_ST	IRQ10_ST	IRQ7_ST	IRQ4_ST	IRQ3_ST	
IRQX ST	Event flag on IRQx interrupt line of ISA bus controller of CPU, '1' – there was an									

IRQx\_ST <u>Event flag on IRQx interrupt line of ISA bus controller of CPU.</u> '1' – there was an interrupt, '0' – there was no interrupt.

IRQx\_EN <u>Reset / permission of setting a flag of IRQx interrupt.</u> Permit – '1', prohibit – '0' (by default, after power on or reset).



#### Attention!

After each interrupt generation on 'IRQx' events it is required to reset a relevant 'IRQx\_EN' interrupt flag by consecutive writing of '0', and then '1' into the relevant bit of interrupt permission. If this is not done, there will be no further settings of event flags.

### 2.8.4 Register of control / system interrupts condition

Enables / prohibits to use external signals when generating an interrupt of NMI CPU, "SYSTEM EVENT" signal during writing to the port. The port also enables to determine a hardware source of NMI and "SYSTEM EVENT".

Address	Action	Action Bits							
Address	Action	7	6	5	4	3	2	1	0
BA+05h	Writing	IOCHK_EN	PFO_EN	WDO_EN	EXT_EN	-	-	SE_NMI_EN	NMI_EN
BA+05h	Reading	IOCHK	PFO	WDO	EXT	-	-	SE_NMI_EN	NMI_EN
IOCHK_E	IOCHK_EN Switching 'ISA_IOCHK#' to the line of NMI CPU. Permit – '1', prohibit – '0'.								
PFO_EN	<u>Switch</u>	ning 'Power	Fail' to th	<u>e line 'SY</u>	STEM E	<u>/ENT'.</u> Pe	ermit – '1'	, prohibit – '	0'.
WDO_EN	<u>Switch</u>	Switching 'WatchDog Timeout' to the line 'SYSTEM EVENT'. Permit – '1', prohibit – '0'.							
EXT_EN	<u>Switch</u>	Switching 'RMTRES' to the line 'SYSTEM EVENT'. Permit – '1', prohibit – '0'.							
SE_NMI_	EN <u>Switch</u>	Switching 'SYSTEM EVENT' to the line of NMI CPU. Permit – '1', prohibit – '0'.							
NMI_EN	'ISA_I		"SYSTEN	I EVENT'	' – during	writing '1		CPU from ion – during	writing '0'
	,	s case, the l				,			
IOCHK	<u>'ISA_I</u>	OCHK#' inc	licator - '1	': active le	evel of 'IS	A_IOCH	<#' signal		
PFO		<u>'POWER FAIL' indicator</u> - '1': reduction of input power supply "+5V" lower than the level of 4.65 V							
WDO		VATCHDOG Timeout' indicator - '1': actuation of the watchdog timer (WDT2) tegrated into the supervisor.							
EXT	'RMTF	<u>RMTRES'</u> indicator - '1': external source of reset/interrupt (XP17-XP18).							



#### Attention!

"SYSTEM EVENT" is generated over "or" from the following sources:

– "Power Fail" (reduction of power supply voltage value down to the level of 4.65 V),

- "WatchDog Timeout" (actuation of the external watchdog timer),

- "RMTRES" (external source of reset / interrupt XP17 / XP18).

Signal of NMI CPU is generated over "or" from the "SYSTEM EVENT" and "ISA\_IOCHK" sources.



#### Attention!

<u>After each interrupt generation on "ISA\_IOCHK#', 'POWER FAIL',</u> 'WATCHDOG Timeout', 'RMTRES' events it is required to reset a relevant interrupt flag by consecutive writing of '0', and then '1' into the relevant bit of interrupt permission. If this is not done, there will be no further generation of interrupts from this port.

E.g., after generation of interrupt over 'RMTRES' event, in the interrupt handler it is required to first reset the 'EXT\_EN' flag in '0', and then set it into '1'.

## 2.8.5 Register of interrupts control of ISA bus controller

Sets the source of interrupts on lines IRQ3, IRQ4, IRQ7, IRQ10, IRQ11, IRQ12, IRQ15 of the CPU. Each line makes it possible to independently connect ISA bus interrupts (IRQ3, IRQ4, IRQ7, IRQ10, IRQ11, IRQ12, IRQ15), as well as the "SYSTEM EVENT" (external source of interrupts, Power Fail event, actuation of watchdog timer).

	Addrose	Action	Bits							
	Address	Action	7	6	5	4	3	2	1	0
	BA+06h	write/read	i15SE	i15SEL[1:0]		EL[1:0]	i11SEL[1:0]		i7SEL[1:0]	
	BA+07h	write/read	i3SEI	_[1:0]	i4SEI	L[1:0]	i10SE	EL[1:0]	-	ISAE
i	15SEL[1:0]		<u>Code of IRQ15 line selector</u> . Possible options: ISA\$IRQ15 (b'00, by default); ISA\$IRQ7 (b'01); ISA\$IRQ3 (b'10);"SYSTEM EVENT" (b'11).							
i	12SEL[1:0]	ISA\$IRQ3 (b'01); ISA\$IRQ4 (b'10); "SYSTEM EVENT" (b'11).								
i	11SEL[1:0]	<u>Code of IRQ11 line selector</u> . Possible options: ISA\$IRQ11 (b'00, by default); ISA\$IRQ7 (b'01); ISA\$IRQ4 (b'10); "SYSTEM EVENT" (b'11).								
ï	7SEL[1:0]	<u>Code of IRQ7 line selector</u> . Possible options: ISA\$IRQ7 (b'00, by default) ; RSVD (b'01); RSVD (b'10); "SYSTEM EVENT" (b'11).								
i:	3SEL[1:0]	<u>Code of IRC</u> (b'01); RSV			•	otions: IS	A\$IRQ3 (	b'00, by d	efault) ; R	SVD
i	4SEL[1:0]	<u>Code of IRC</u> (b'01); RSV			•	otions: IS	A\$IRQ4 (	b'00, by d	efault) ; R	SVD
i	10SEL[1:0]		<u>Code of IRQ10 line selector</u> . Possible options: ISA\$IRQ10 (b'00, by default) ; ISA\$IRQ7 (b'01); ISA\$IRQ3 (b'10); "SYSTEM EVENT" (b'11).							
ļ	SAE	Control of buffer elements of ISA bus. '0': deactivated (outputs in 'Z'-condition). '1': buffer elements of ISA bus are activated (by default during power on or reset). If buffer elements are deactivated, no devices on external ISA bus will be available!								
*	* RSVD – Reserved.									

The port is also used for activation/deactivation of buffer elements of ISA bus.

### 2.8.6 Control register of page access to NV SRAM 128 KB

Address	Action	Bits							
Address	Action	7	6	5	4	3	2	1	0
BA+0Ch	Writing	-	-	-	-	-	BNK2	BNK1	BNK0
BA+0Ch	Reading	-	-	-	-	-	BNK2	BNK1	BNK0

Enables a program control of NV SRAM active page number.

BNK[2:0] <u>SRAM active page number.</u> Page size: 16 KB. Base window address is selected in BIOS Setup settings (by default: D8000h).

### 2.8.7 Code register of XCS05 version

Code of the version number of XCS05 matrix diagram is available over reading via byte port with BA+0Eh address.

Address	Action	Bits									
Address	Action	7	6	5	4	3	2	1	0		
BA+0Eh	Reading		Ver_05				Rev_05				
BA+0Fh	Reading			-			-	-			

Ver\_05 - numeric code of the version number of XCS05 matrix diagram;

Rev\_05 – numeric code of the revision number of XCS05 matrix diagram.

## 2.9 Table of module connector contacts <sup>13</sup>

## 2.9.1 Table of XP1 connector contacts: Compact Flash

Table 2-32: Purpose of XP1 connector contacts: Compact Flash

XP2: N7E50-M	516RB-50 (3M)		
Contact #	Function	Contact #	Function
1	GND	2	D3
3	D4	4	D5
5	D6	6	D7
7	CSO#	8	A10
9	ATA_SEL#	10	А9
11	A8	12	A7
13	VCC (3.3V)	14	A6
15	A5	16	A4
17	A3	18	A2
19	A1	20	A0
21	D0	22	D1
23	D2	24	IOCS16#
25	CD2#	26	CD1#
27	D11	28	D12
29	D13	30	D14
31	D15	32	CS1#
33	VS1#	34	IORD#
35	IOWR#	36	WE#
37	INTRQ#	38	VCC (3.3V)
39	CSEL#	40	-
41	RESET#	42	IORDY
43	INPACK#	44	REG#
45	DASP#	46	PDIAG#
47	D8	48	D9
49	D10	50	GND

 $<sup>^{\</sup>rm 13}$  From this point on: symbol  ${\it \#}$  in the name of the signal - active level of log. "0".

#### Table of XP2 connector contacts: Analog RGB port 2.9.2

XP2: 98424-G52-10LF, FCI						
Contact #	Function	Contact #	Function			
1	RED	2	GND			
3	GREEN	4	GND			
5	BLUE	6	GND			
7	HSYNC	8	VSYNC			
9	DDC_SCL	10	DDC_SDA			

Table 2-33: Purpose of XP2 connector contacts: IDE port

#### Table of XP3, XP4 connectors contacts: COM1, COM2 (RS-422/485) 2.9.3

XP3: 733-335 (WAGO), 5 contacts, pitch of 2.5 mm							
Contact #	Function 1	Function 1 Function 2					
1	TX+	RTXD+					
2	TX-	RTXD-					
3	RX+	-					
4	RX						
5	GNDS1 <sup>14</sup>						

Table	2-34:	Purpose of XP3 connector contacts: COM1 (RS-422/485)	
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Table 2	2-35:	Purpose of XP4 connector contacts: COM2 (RS-422/485)

XP4: 733-335 (WAGO), 5 contacts, pitch of 2.5 mm							
Contact #	Function 1	Function 1 Function 2					
1	TX+	RTXD+					
2	TX-	RTXD-					
3	RX+	-					
4	RX						
5	GNDS2 <sup>15</sup>						

<sup>&</sup>lt;sup>14</sup> Ground, isolated from the system (isolation from the system: 500 V). <sup>15</sup> Ground, isolated from the system (isolation from the system: 500 V).

## 2.9.4 Table of XP5 connector contacts: LPT port

XP5: IDC-26 2.54 mm (5104338-6, AMP)			
Contact #	Function	Contact #	Function
1	STB#	2	AFD#
3	PD0	4	ERR#
5	PD1	6	INIT#
7	PD2	8	SLCTIN#
9	PD3	10	GND
11	PD4	12	GND
13	PD5	14	GND
15	PD6	16	GND
17	PD7	18	GND
19	ACK#	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT#	26	+5V_EXTP

 Table 2-36:
 Purpose of XP5 connector contacts: LPT port

#### 2.9.5 Table of XP6, XP7 connectors contacts: COM3, COM4 (RS-232)

XP6, XP7: IDC-10, pitch of 2.54 mm (5104338-1, AMP)				
Contact #	Function	Contact #	Function	
1	DCD#	2	DSR#	
3	RXD	4	RTS#	
5	TXD	6	CTS#	
7	DTR#	8	RI#	
9	GND	10	+5V_EXTR	

#### Table 2-37: Purpose of XP6, XP7 connector contacts: COM3, COM4

#### 2.9.6 Table of XP8 connector contacts: PS/2 port of keyboard / mouse

 Table 2-38:
 Purpose of XP8 connector contacts: PS/2 port of keyboard/mouse

XP3: B 5B-PH-KL	XP3: B 5B-PH-KL (JST), 5 contacts, pitch of 2 mm		
Contact #	Function		
1	KBD_CLK		
2	KBD_DAT		
3	MS_CLK		
4	GND		
5	+5V_EXTK		
6	MS_DAT		

## 2.9.7 Table of XP10 connector contacts: GPIO port

 Table 2-39:
 Purpose of XP10 connector contacts

XP10: 98424-G52-10LF, FCI			
Contact #	Function	Contact #	Function
1	GPIO[0]	2	GPIO[1]
3	GPIO[2]	4	GPIO[3]
5	GPIO[4]	6	GPIO[5]
7	GPIO[6]	8	GPIO[7]
9	+5VEXT	10	GND

## 2.9.8 Table of XP14 connector contacts: buzzer

XP14: B 2B-PH-KL (JST), pitch of 2 mm		
Contact #	Function	
1	+5V_EXTL	
2	SPK_DRV	

# 2.9.9 Table of XP15 connector contacts: connection to KIB98102 (VGA,TFT,AUDIO,KB,MS)

Contact #	Function	Description	Contact #	Function	Description
1	KB_DAT	Data, KBD	2	+5V_EXTM	Power supply (PS/2)
3	KB_CLK	Clock, KBD	4	MS_CLK	Data, MOUSE
5	GND	Power supply	6	MS_DAT	Clock, MOUSE
7	+3.3/+5V	Power supply (TFT)	8	+3.3/+5V	Power supply (TFT)
9	FP_BLUE0	Data, TFT	10	FP_BLUE1	Data, TFT
11	FP_BLUE2	Data, TFT	12	FP_BLUE3	Data, TFT
13	FP_BLUE4	Data, TFT	14	FP_BLUE5	Data, TFT
15	GND	Power supply	16	FP_GREEN0	Data, TFT
17	FP_GREEN1	Data, TFT	18	FP_GREEN2	Data, TFT
19	FP_GREEN3	Data, TFT	20	FP_GREEN4	Data, TFT
21	FP_GREEN5	Data, TFT	22	GND	Power supply
23	FP_RED0	Data, TFT	24	FP_RED1	Data, TFT
25	FP_RED2	Data, TFT	26	FP_RED3	Data, TFT
27	FP_RED4	Data, TFT	28	FP_RED5	Data, TFT
29	GND	Power supply	30	FP_CLK	Clock, TFT
31	GND	Power supply	32	FP_DISPEN	Control, TFT
33	GND	Power supply	34	FP_HSYNC	Control, TFT
35	FP_BKTLEN	Control, TFT	36	FP_VSYNC	Control, TFT
37	FP_VDDEN	Control, TFT	38	GND	Power supply
39	CRT_RED	Data, VGA	40	GND	Power supply
41	CRT_BLUE	Data, VGA	42	GND	Power supply
43	CRT_GREEN	Data, VGA	44	GND	Power supply
45	DDC_SDA	Service, VGA	46	CRT_HSYNC	Control, VGA
47	CRT_VSYNC	Control, VGA	48	DDC_SCL	Service, VGA
49	GND	Power supply	50	VCCA	Power supply, Audio
51	LINEOUT_L	Audio	52	GND	Power supply, Audio
53	LINEOUT_R	Audio	54	GND	Power supply, Audio
55	LINEIN_L	Audio	56	GND	Power supply, Audio
57	LINEIN_R	Audio	58	GND	Power supply, Audio
59	MICIN	Audio	60	GND	Power supply, Audio

#### Table 2-41: Purpose of XP15 connector contacts: KIB98102 (VGA,TFT,AUDIO,KB,MS)

## 2.9.10 Table of XP16 connector contacts: connection to KIB98201 (IDE, LPT)

ontact #	Function	Description	Contact #	Function	Description
1	RxD	Data, COM9	2	-	
3	TxD	Data, COM9	4	+5VEXTD	Power supply
5	LPT_STB#	Control, LPT	6	LPT_AFD#	Control, LPT
7	LPT_D0	Data, LPT	8	LPT_ERR#	Control, LPT
9	LPT_D1	Data, LPT	10	LPT_INIT#	Control, LPT
11	LPT_D2	Data, LPT	12	LPT_SLIN#	Control, LPT
13	LPT_D3	Data, LPT	14	GND	Power supply
15	LPT_D4	Data, LPT	16	LPT_D5	Data, LPT
17	LPT_D6	Data, LPT	18	LPT_D7	Data, LPT
19	GND	Power supply	20	LPT_ACK#	Control, LPT
21	LPT_BUSY	Control, LPT	22	LPT_PE	Control, LPT
23	LPT_SLCT#	Control, LPT	24	GND	Power supply
25	-		26	-	
27	-		28	-	
29	-		30	-	
31	-		32	-	
33	-		34	-	
35	-		36	-	
37	GND	Power supply	38	IDE_RST#	Control, IDE
39	GND	Power supply	40	IDE_D[7]	Data, IDE
41	IDE_D[8]	Data, IDE	42	IDE_D[6]	Data, IDE
43	IDE_D[9]	Data, IDE	44	IDE_D[5]	Data, IDE
45	IDE_D[10]	Data, IDE	46	IDE_D[4]	Data, IDE
47	IDE_D[11]	Data, IDE	48	GND	Power supply
49	IDE_D[3]	Data, IDE	50	IDE_D[12]	Data, IDE
51	IDE_D[2]	Data, IDE	52	IDE_D[13]	Data, IDE
53	IDE_D[1]	Data, IDE	54	IDE_D[14]	Data, IDE
55	IDE_D[0]	Data, IDE	56	IDE_D[15]	Data, IDE
57	GND	Power supply	58	IDE_DRQ#	Control, IDE
59	IDE_IOW#	Control, IDE	60	GND	Power supply
61	IDE_IOR#	Control, IDE	62	GND	Power supply
63	IDE_IORDY#	Control, IDE	64	IDE_DACK#	Control, IDE
65	IDE_INT#	Control, IDE	66	IDE_BA[1]	Control, IDE
67	IDE_BA[0]	Control, IDE	68	IDE_BA[2]	Control, IDE
69	IDE_CS0#	Control, IDE	70	IDE_CS1#	Control, IDE
71	+5VEXTD	Power supply	72	+5VEXTD	Power supply

#### Table 2-42: Purpose of XP16 connector contacts: KIB98201 (IDE,LPTTFT,AUDIO,KB,MS)

### 2.9.11 Table of XP17-XP18 connector contacts: remote reset / interrupt

Table 2-43: Purpose of XP17, XP18 connector contacts: ports of isolated remote reset / interrupt

XP17: B 2B-PH-KL (JST), pitch of 2 mm	
Contact #	Function
1	RMTRES+
2	RMTRES-

XP18: B 2B-PH-KL (JST), pitch of 2 mm	
Contact #	Function
1	RMTRES
2 GNDS1	

### 2.9.12 Table of XP20 connector contacts: module power supply

Table 2-44:	Purpose of XP20 connector contacts: module power supply

XP20: 22-27-2041, pitch of 2.54 mm (Molex)	
Contact #	Function
1	+12V
2	GND
3	GND
4	+5V

#### 2.9.13 Table of XP21 connector contacts: USB2/3 ports

 Table 2-45:
 Purpose of XP21 connector contacts: USB2/3 ports

XP21: IDC1	XP21: IDC10, pitch of 2 mm (98424-G52-10LF, FCI)					
Contact #	Purpose	Configuration		Contact #	Purpose	Configuration
1	+5 V @ 0.5A	Power supply		2	+5 V @ 0.5A	Power supply
3	D-	Data		4	D-	Data
5	D+	Data		6	D+	Data
7	GND	Power supply		8	GND	Power supply
9	-			10	-	

## 2.9.14 Table of XS4 connector contacts: PC/104 (ISA 8/16 bit)

XS4: Conne	XS4: Connector of PC/104 bus extension (2x32 + 2x20 contacts), lines A, B					
Contact #	Purpose	Configuration		Contact #	Purpose	Configuration
A1	IOCHK#	Input		B1	GND	Power supply
A2	SD7	Input/Output		B2	RESET	Output
A3	SD6	Input/Output		B3	+5V	Input
A4	SD5	Input/Output		B4	IRQ9	Input
A5	SD4	Input/Output		B5	-	
A6	SD3	Input/Output		B6	DRQ2	Input
A7	SD2	Input/Output		B7	-12V	Power supply
A8	SD1	Input/Output		B8	0WS#	Input
A9	SD0	Input/Output		B9	+12V	Power supply
A10	IOCHRDY	Input		B10	GND	Power supply
A11	AEN	Output		B11	SMEMW#	Output
A12	SA19	Output		B12	SMEMR#	Output
A13	SA18	Output		B13	IOW#	Output
A14	SA17	Output		B14	IOR#	Output
A15	SA16	Output		B15	DACK3#	Output
A16	SA15	Output		B16	DRQ3	Input
A17	SA14	Output		B17	DACK1#	Output
A18	SA13	Output		B18	DRQ1	Input
A19	SA12	Output		B19	DACK0#	Output
A20	SA11	Output		B20	BCLK	Output
A21	SA10	Output		B21	IRQ7	Input
A22	SA9	Output		B22	IRQ6	Input
A23	SA8	Output		B23	IRQ5	Input
A24	SA7	Output		B24	IRQ4	Input
A25	SA6	Output		B25	IRQ3	Input
A26	SA5	Output		B26	DACK2#	Output
A27	SA4	Output		B27	ТС	Output
A28	SA3	Output		B28	BALE#	Output
A29	SA2	Output		B29	+5V	Power supply
A30	SA1	Output		B30	OSC	Output
A31	SA0	Output		B31	GND	Power supply
A32	GND	Power supply		B32	GND	Power supply

#### Table 2-46: Purpose of XS4 connector contacts: PC/104 (ISA 8/16 bit) lines A, B

Contact #	Purpose	Configuration	Contact #	Purpose	Configuration
C0	GND	Power supply	D0	GND	Power supply
C1	SBHE#	Output	D1	MEMCS16#	Input
C2	LA23	Output	D2	IOCS16#	Input
C3	LA22	Output	D3	IRQ10	Input
C4	LA21	Output	D4	IRQ11	Input
C5	LA20	Output	D5	IRQ12	Input
C6	LA19	Output	D6	IRQ15	Input
C7	LA18	Output	D7	IRQ14	Input
C8	LA17	Output	D8	DACK0#	Output
С9	MEMR#	Output	D9	DRQ0	Input
C10	MEMW#	Output	D10	DACK5#	Output
C11	SD8	Input/Output	D11	DRQ5	Input
C12	SD9	Input/Output	D12	DACK6#	Output
C13	SD10	Input/Output	D13	DRQ6	Input
C14	SD11	Input/Output	D14	DACK7#	Output
C15	SD12	Input/Output	D15	DRQ7	Input
C16	SD13	Input/Output	D16	+5V	Power supply
C17	SD14	Input/Output	D17	-	
C18	SD15	Input/Output	D18	GND	Power supply
C19	-		D19	GND	Power supply

### Table 2-47: Purpose of XS4 connector contacts: PC/104 (ISA 8/16 bit) lines C, D

## 2.9.15 Table of XS6 connector contacts: MicroPC ISA 8 bit

Contact #	Purpose	Configuration	Contact #	Purpose	Configuration
A1	IOCHK#	Input	B1	GND	Power supply
A2	SD7	Input/Output	B2	RESET	Output
A3	SD6	Input/Output	B3	+5V	Input
A4	SD5	Input/Output	B4	IRQ9	Input
A5	SD4	Input/Output	B5	-	
A6	SD3	Input/Output	B6	DRQ2	Input
A7	SD2	Input/Output	B7	-12V	Power supply
A8	SD1	Input/Output	B8	0WS#	Input
А9	SD0	Input/Output	B9	+12V	Power supply
A10	IOCHRDY	Input	B10	GND	Power supply
A11	AEN	Output	B11	SMEMW#	Output
A12	SA19	Output	B12	SMEMR#	Output
A13	SA18	Output	B13	IOW#	Output
A14	SA17	Output	B14	IOR#	Output
A15	SA16	Output	B15	DACK3#	Output
A16	SA15	Output	B16	DRQ3	Input
A17	SA14	Output	B17	DACK1#	Output
A18	SA13	Output	B18	DRQ1	Input
A19	SA12	Output	B19	DACK0#	Output
A20	SA11	Output	B20	BCLK	Output
A21	SA10	Output	B21	IRQ7	Input
A22	SA9	Output	B22	IRQ6	Input
A23	SA8	Output	B23	IRQ5	Input
A24	SA7	Output	B24	IRQ4	Input
A25	SA6	Output	B25	IRQ3	Input
A26	SA5	Output	B26	DACK2#	Output
A27	SA4	Output	B27	тс	Output
A28	SA3	Output	B28	BALE#	Output
A29	SA2	Output	B29	+5V	Power supply
A30	SA1	Output	B30	OSC	Output
A31	SA0	Output	B31	GND	Power supply

#### Table 2-48: Purpose of XS6 connector contacts: MicroPC (ISA 8 bit)

# **SECTION 3**

# **INSTALLATION AND CONFIGURATION**

# **3** INSTALLATION AND CONFIGURATION

The module can be installed into **MicroPC** mounting baskets, **ISA** - compatible mounting frames or connected by a **flexible ribbon cable** with edge connectors to other modules.



#### Attention!

Installation into **PC slots** can bring module out of operation.



#### Attention!

The module contains sensitive components. Installation, removal, connection of module with its power on, as well as a static discharge from your hands can damage the module.



#### Attention!

During installation it is required to observe the proper orientation of module connectors towards connectors of the backplane.



Fig. 3-1: Diagram of CPC152 module connection to backplane

It is also possible to extend functionalities by installing modules in **PC/104 format (ISA 8/16 bit)**. It is permitted to install no more than 4 PC/104 extension modules.

Conventional view of installation and connection of extension modules in PC/104 format is shown in the figure.

Fig. 3-2: Conventional view of installation and connection of extension modules in PC/104 format



## 3.1 Installation of module switches

For module hardware configuration, it is possible to use the group of switches, which general description is specified in the table below.

Switches	Description
X1	Permission / prohibition of switching to BIOS backup copy
X2	Service jumper (do not close!)
X3, X4, X5	Purpose of IDE integrated devices: Master or Slave
X6	Selection of power supply voltage for LCD panel (connection via KIB98102, XP15)
X7, X8, X9	Switching of Power Fail signals, watchdog timer (WDT2) actuation, of remote reset line to CPU hardware reset line
X10 – X13	Binding of COM1 (RS-422/485) lines and connection of conforming resistors
X14	Selection of COM1 operation mode (RS-422/485): rate of rise limitation
X15 – X18	Binding COM2 lines (RS-422/485) and connection of conforming resistors
X19	Selection of COM2 operation mode (RS-422/485): rate of rise limitation
X23	Setting actuation voltage level of remote reset
X40	Connection of nonvolatile RAM 128 KB

Table 3-1:	Purpose of switched for module configuration

## 3.1.1 Switching to BIOS booting from the main / standby source

Table 3-2:         Switching to BIOS booting from the main / standby set	ource
--	-------

Jumper	Description
X1 [1-2]	Prohibition of automatic switching to BIOS backup copy (in this case there will be no automatic switching to the backup copy)
X1 [0-0]	Mode of automatic switching to booting from BIOS backup copy

## 3.1.2 Purpose of IDE integrated devices: Master or Slave

Jumper	Description
X3 [1-2]	
X4 [0-0]	Flash-drive: Primary Master Compact Flash: Primary Slave
X5 [0-0]	
X3 [0-0]	
X4 [1-2]	Flash-drive: Primary Slave Compact Flash: Primary Master
X5 [0-0]	
X3 [0-0]	
X4 [1-2]	Flash-drive: deactivated Compact Flash: Primary Master
X5 [1-2]	
X3 [0-0]	
X4 [0-0]	Flash-drive: deactivated Compact Flash: Primary Slave
X5 [1-2]	

#### Table 3-3: Purpose of IDE integrated devices: Master or Slave

# 3.1.3 Selection of power supply voltage for LCD panel (connection via KIB98102, XP15)

#### Table 3-4: Selection of power supply voltage for LCD panel (connection via KIB98102, XP15)

Jumper	Description
X6[1-2]	There was a selection of voltage of +5 V for power supply of LCD panel, connected via KIB98102 module (XP15 connector of CPC152 module)
X6[2-3]	There was a selection of voltage of +3.3 V for power supply of LCD-panel, connected via KIB98102 module (XP15 connector of CPC152 module)

# 3.1.4 Switching of Power Fail signals, watchdog timer actuation, remote access to the line of CPU hardware reset

## Table 3-5: Switching of Power Fail signals, watchdog timer actuation, remote access to the line of CPU hardware reset

Jumper	Description	
X7[1-2]	Switching of Power Fail signal to the line of CPU hardware reset	
X8[1-2]	Switching of watchdog timer (WDT2) actuation signal to the line of CPU hardware reset (used for automatic switching to the BIOS backup copy in case of a boot failure while booting from the main copy)	
X9[1-2]	Switching of external signal of a remote reset / interrupt (from XP17, XP18 connectors) to the line of CPU hardware reset	

## 3.1.5 Binding and matching of COM1 port lines (RS-422/485)

#### Table 3-6: Binding and matching of COM1 port (RS-422/485)

Jumper	Description
X10 [1-2]	Signal +TX / +RTXD via resistor 680 Ohm is brought up to the isolated power supply voltage of +5VS1 for generation of 200 mW displacement on Y/Z lines
X11 [1-2]	Signal -TX / -RTXD via resistor 680 Ohm is brought up to the GNDS1 isolated ground.
X10 [1-2] & X11 [1-2]	Connection of conforming resistor 120 Ohm between the lines ±TX / ±RTxD
X12 [1-2]	Selection of rate of rise mode limitation of output signal. In this case, the exchange speed is limited by the value of 250 Kb/sec.

### 3.1.6 Selection of COM1 port operation mode (RS-422/485)

#### Table 3-7: Selection of COM1 port operation mode (RS-422/485)

Jumper	Description
X13 [1-2] & X14 [1-2]	Half-duplex mode
X13 [0-0] & X14 [0-0] <sup>16</sup>	Full-duplex mode

### 3.1.7 Binding and matching of COM2 port lines (RS-422/485)

#### Table 3-8: Binding and matching of COM2 lines (RS-422/485)

Jumper	Description
X15 [1-2]	Signal +TX / +RTXD via resistor 680 Ohm is brought up to the isolated power supply voltage +5VS2 for generating 200 mW displacement on Y/Z lines
X16 [1-2]	Signal -TX / -RTXD via resistor 680 Ohm is brought up to the GNDS2 isolated ground.
X15 [1-2] & X16 [1-2]	Connection of conforming resistor 120 Ohm between the lines ±TX / ±RTxD
X17 [1-2]	Selection of rate of rise mode limitation of output signal. In this case, the exchange speed is limited by the value of 250 Kb/sec.

#### 3.1.8 Selection of COM2 port operation mode (RS-422/485)

#### Table 3-9: Selection of COM2 port operation mode (RS-422/485)

Jumper	Description
X18 [1-2] & X19 [1-2]	Half-duplex mode
X18 [0-0] & X19 [0-0]	Full-duplex mode

<sup>&</sup>lt;sup>16</sup> From this point on: write of "Xnn[0-0]" view means that the specified jumper is open.
# 3.1.9 Setting the voltage level of remote reset actuation (XP17)

 Table 3-10:
 Setting the voltage level of remote reset actuation (XP17)

Jumper	Description
X23[1-2]	Range of actuation voltages: 3 V 15 V
X23[2-3]	Range of actuation voltages: 10 V 30 V

# 3.1.10 Connection of nonvolatile RAM

Table 3-11:	Connection of integrated nonvolatile RAM
-------------	--

Jumper	Description
X40 [1-2]	Integrated nonvolatile RAM of 128 KB is connected

# 3.2 Configuration of module's parameters (BIOS SETUP)

Parameters of CPC152 module configuration are stored in the internal nonvolatile memory (FRAM) and can be changed in BIOS Setup.

Setting configuration parameters for CPC152 is carried out during module's booting while pressing the *<Del>* button on the keyboard, connected to the PS/2 or USB port, by *<F4>* button on the keyboard of the remote terminal, when connection the module via a console serial COM-port.

Description of BIOS Setup settings is given in Section 5 "Basic Input/Output System (BIOS)".

# **SECTION 4**

# **INTENDED USE OF CPC152**

# 4 Intended use of CPC152

# 4.1 Basic software

At the time of delivery, the integrated FLASH-drive of CPC152 contains programs, ensuring operating readiness of the device:

- integrated FreeDOS operating system
- service program of data uploading/downloading (ftrans.exe)
- system utility for transfer of system files (sys.com)

Кроме того, в комплект поставки модуля входит диск с документацией, утилитами для модификации FLASH BIOS и примерами программирования.

The latest versions of documents, BIOS and utilities can be found at <u>ftp://ftp.prosoft.ru/pub/Hardware/Fastwel/CPx/CPC152/</u>.

# 4.2 Setting connection between PC and CPC152

For setting connection between the PC and CPC152 module it is required:

- When the power of PC and CPC152 is off, connect the cable VTC-9F with a 0-modem adapter to PC COM-port and XP6 / XP7connector of the CPC152 module (by default, COM3 is set as a console one). For connection to COM3 (XP6) and COM4 ports (XP7), ACS00005 adapter cable is used (1 pcs. included into the delivery checklist).
- 2. Install the package of terminal software SmartLINK or any other equivalent program with the following sequence link parameters:
  - PC port (COM1 / COM2)
  - 8 bit data
  - 1x stop bit
  - without even-parity check
  - exchange rate of 115200 Kb/sec
- 3. Switch on the power and press the RESET button, if it is not necessary to fulfill items 1, 2 and the power is on. In case the connection has been set successfully, after the booting of operating system, on PC screen there will be a line of DOS invitation: C:>
- 4. For booting of operating system without execution of commands of **CONFIG.SYS** and **AUTOEXEC.BAT** files, after power on or RESET it is required to press combinations of <Ctrl-B> or <Ctrl-C> keys on PC keyboard for step-by-step execution of commands.

# 4.3 Module operation wit AT-keyboard and CRT-display/TFT-panel

When connecting an AT-keyboard and CRT-display or TFT-panel to the module (via KIB98102 interface board using an integrated video controller or by using an external MicroPC or PC/104 video adapter) the CPC152 module can be used as a standard AT (x86) - compatible PC. In this case, start and debugging of programs is carried out as usual and is not described here.

# 4.4 Loading files with FTRANS.EXE program

File exchange between PC and CPC152 module is performed using the **ftrans.exe** utility. For exchanging files it is required to carry out the following activities:

- set the connection between PC and CPC152;
- start the **ftrans.exe** program with the required parameters (see integrated program help);
- within no more than 50 seconds from the start of ftrans.exe program, to carry out the required activities (specify the transfer direction, file name etc.) in SmartLINK program or other terminal program (see program description).

In order to use the **FTRANS** utility for remote loading of files via COM3 / COM4 ports, it is required to specify their base addresses 3F8h and 2F8h in BIOS Setup settings, which corresponds to the standard allocation of addresses for COM1 / COM2 (set by default in BIOS Setup settings).

# 4.5 Interface BIOS SOC Vortex86DX for reading serial number, MACaddress

for storing system parameters, FRAM array is used. In order to store the whole system information, a volume equal to 1KB is used (it can be subject to minor changes depending on BIOS revision).

### 4.5.1 Array structure:

_FRAM	STRUCT		
	db	256 dup (0)	; Reserve for storage of CMOS copy
dSerNum	dd	0	; Module serial number
wMac dw	-1,-1,-1		; MAC-address of integrated LAN
FRAM	ENDS		

Parameter values, transferred in CPU registers, are given below. In case of a wrong number of (AL) function, AX = -1 (0FFFh) is returned.

### 4.5.2 Obtaining module serial number.

Input: AL = 6

Output: AX = Result code (0 - no error)

CX:DX = serial number.

### 4.5.3 Reading of MAC address of integrated LAN-control from the FRAM area.

Input: AL = 8

AX = Result code (0 - no error)

Output: SI:CX:DX = MAC-address.

The function returns the value, stored in the area of MAC-address of FRAM. Actual value used by the controller, can vary if it was overwritten to the registers of controller by application software.

# 4.6 Interface BIOS SOC Vortex86DX for reading/writing to FRAM

Integrated nonvolatile memory FRAM is also available for storing user data.

In order to call the FRAM reading/writing service, **INT 17H** interrupt is used with a parameter in the AH = 0ADh register.

Values of other parameters, transferred in CPU registers, are described below.

In case of a wrong number of (AL) function, AX = -1 (0FFFh) is returned.

#### 4.6.1 Reading user data from FRAM.

Input:AL = 0ChBX = address of data start in the user area of FRAMCX = number of readable bytesDS:DX = indicator to the reading bufferOutput:AX = result code (0 - no error, -2 (0FFFEh) – parameter error, wrong address)BX = maximum permissible address (size of user area -1)CX = number of actual bytes read

This function reads the specified bytes of FRAM user area into the buffer of calling program.

### 4.6.2 Writing user data from FRAM.

- - -

. .

.

Input:	AL = 0Dh
	BX = address of data start in the user area of FRAM
	CX = number of bytes written
	DS:DX = indicator to the data written
Output:	AX = result code (0 - no error, -2 (0FFFEh) – parameter error, wrong address)
	BX = maximum permissible address (size of user area -1)
	CX = number of actual bytes written

\* This function writes data to FRAM user area.

# 4.7 Service utility programs

This chapter describes a set of drivers for operation with I/O devices, connected to CPC152 module.

### 4.7.1 XFLASH.EXE utility (upgrade of BIOS backup copy)

The **xflash.exe** program is designed for modifying BIOS with writing into the integrated SPI-Flash of the CPU in the CPC152 module. A prerequisite of the upgrade is booting from BIOS backup copy.

In order to modify BIOS it is required to start the program with "w" key and specify BIOS file name as parameter:

xflash w bios.bin

### 4.7.2 VXDXBIOS.EXE utility (upgrade of BIOS main copy)

The vxdxbios.exe program is designed for modifying BIOS with writing to the external FLASHmemory (from PLCCC32 socket) in the CPC152 module. In this case it is required to properly install the jumpers, responsible for switching the BIOS booting source.

In order to modify BIOS it is required to start the program and specify BIOS file name as parameter:

#### vxdxbios bios.bin



#### Attention!

After BIOS upgrade, it is required to enter the BIOS Setup menu and load optimum values, since CMOS structure can distinguish from various BIOS versions (see <u>Section 5 Basic Input/Output System (BIOS)</u> of this User Manual).

After that BIOS Setup settings can be changed.

### 4.7.3 CMOS\_RST.EXE utility (remote reset of BIOS settings)

The **CMOS\_RST.EXE** program is designed for reset of BIOS settings to the default state (similarly to the effect of item BIOS Setup "Load Optimal Defaults"). For reset of the setting using **CMOS\_RST.EXE** program it is required to connect COM3 or COM4 port of CPC152 module with COM port of the PC by a null modem cable and turn on the module power supply (settings will be reset and written to the CMOS and FRAM, then a hardware reset will be carried out automatically and module will be started with default settings). The used PC should be equipped with installed OS Win32 (WinNT/2000/XP).

Syntax:

#### cmos\_rst.exe [COM]

where

**[COM]** – number of the COM-port used in PC, COM1 by default.

# **SECTION 5**

# **BASIC INPUT/OUTPUT SYSTEM (BIOS)**

# 5 BASIC INPUT/OUTPUT SYSTEM (BIOS)

In order to enter the BIOS Setup, it is required during system booting and at the time of the POST (Power On Self Test) procedure to press the «DEL» button on the keyboard or «F4» button on the keyboard of a console PC (the "Console Redirect" option should be on). Example of the POST procedure screen is shown in Figure 5.1.





Using the BIOS Setup Utility it is possible to change BIOS (Basic Input Output System) parameters and control special modes of module operation. This program uses the system menu for making changes, as well as for activation or deactivation of special functions.

Information fields (highlighted with grey font color) are designed for output of additional information on module and/or module settings and are not available for changing by the user.

When describing menu items, values set by default, are underlined. Information fields should be printed in italics. Setting the wrong values could lead to malfunctions in system operation.

For displaying the menu for selection of a drive, which will be used for booting of operating system, during system booting and at the time of POST procedure it is required to press the "F11" button on keyboard or "F3" button on the keyboard of console PC (the "Console Redirect" option should be on). Example of the menu of boot device selection is given in the figure 5.2.

************************	******
* Please select boot devi	
************	*******
* HDD:PS-SanDisk SDCFB-128	*
	*
*	*
*	*
÷	*
*	*
*	*
*	*
********	******
* * and * to move selecti	
* ENTER to select boot dev	
<ul> <li>ESC to boot using defau</li> </ul>	lts *
* * * * * * * * * * * * * * * * * * * *	*******

Fig. 5-2: Menu of boot device selection

# 5.1 Main

This menu tab contains description of BIOS version, installed CPU and RAM. There are also two items, responsible for adjustment of current date and time. Screen of "Main" menu is shown in Figure 5.3, description of items is shown in table 5.1.



	BIOS SETUP UTILITY								
	Main	Advanced	PCIPnP	Boot	Security	Chi	pset	Exit	
*	******	* * * * * * * * * * *	*******	*******	* * * * * * * * * * *	****	****	*****	* * *
*	System (	Dverview				*	Use	[ENTER], [TAB]	*
*	******	* * * * * * * * * * *	*******	*******	* * * * * * * * * * *	*** *	or [	SHIFT-TAB] to	*
*	AMIBIOS					*	sele	ect a field.	*
*	Version	:08.00.1	5			*			*
*	Build Da	ate:07/09/1	3			*	Use	[+] or [-] to	*
*	ID	:3BABTOO	0			*	conf	igure system Time	. *
*	Fastwel	FPGA Firmwa	are			*			*
*	XCSO5 Re	ev.:1.3				*			*
*						*			*
*	Processo	or				*			*
*	Vortex86	5DX A9121				*			*
*	Speed	:600MHz				*			*
*	System 1	Memory				*	*	Select Screen	*
*	256MB at	t 333MHz				*	**	Select Item	*
*						*	+-	Change Field	*
*		Гime		[00:00	:07]	*	Tab	Select Field	*
*	System I	Date		[Tue O	7/09/2013]	*	F1	General Help	*
*						*	F 6	Reset WDT	*
*						*	F10	Save and Exit	*
*						*	ESC	Exit	*
*	******	* * * * * * * * * * *	******	******	* * * * * * * * * * *	****	****	*****	* * *
		v02.61 (	C)Copyrigh	t 1985-20	06, America	n Meg	atren	nds, Inc.	

Table 5-1: Description of "Main" menu

Menu item	Assignment				
AMIBIOS (Information on BIOS version)	Version – current BIOS version Build Date – build date of BIOS ID – BIOS identifier				
Fastwel FPGA Firmware (firmware versions and identifiers of integrated PLDs)	XCS05 Rev. – version of system PLD				
<b>Processor</b> (information field)	Information on CPU installed on the module: <i>Vortex A9121</i> – version of Vortex86DX CPU <i>Speed</i> – CPU clock frequency				
<b>System Memory</b> (information field)	Information on DDR2 SDRAM installed on the module: volume of RAM and frequency of bus operation				
System Time	Current time in format [hour/min/sec]				
System Date	Current date in format [month/day/year]				

# 5.2 Advanced (additional settings)

This menu tab contains items responsible for operation of the soldered ATA Flash Disk controller, Cache-memory of the CPU, IDE bus, console input-output and USB devices. Screen of "Advanced" menu is shown in Figure 5.4, description of items is given in the table 5.2.

		TUP UTILITY			
Main Advanced PCIP		Security	-	Exit	
* * * * * * * * * * * * * * * * * * * *	* * * * * * * * * * * * *	* * * * * * * * * * * * *	******	*****	* 1
Advanced Settings				gure Remote	
*****	* * * * * * * * * * * *	* * * * * * * * * * * * *	*** * Acces	з.	
WARNING: Setting wrong va	alues in bel	ow sections	*		
may cause system	n to malfunc	tion.	*		
			*		
Embedded NAND Flash	[Disal	oled]	*		
Reserve BIOS Switch by WI	DT [Enab	led]	*		
Start Manufacturing Link			*		
			*		
Module Temperature :	53*C		*		
USB Power Overcurrent :	not found		*		
Main/Reserve BIOS :	Main		*		
			* *	Select Screen	
* CPU Configuration			* **	Select Item	
* IDE Configuration			* Enter	Go to Sub Scree	n
* Remote Access Configura			* F1	General Help	
* USB Configuration			* F6	Reset WDT	
			* F10	Save and Exit	
			* ESC	Exit	
			*		
* * * * * * * * * * * * * * * * * * * *	* * * * * * * * * * * *	* * * * * * * * * * * *	* * * * * * * * * * *	* * * * * * * * * * * * * * * * *	*
v02.61 (C)Copv	right 1985-2)	006, America	n Megatrend	s, Inc.	

# Fig. 5-4:Screen of "Advanced" menu

 Table 5-2:
 Description of "Advanced" menu (additional settings)

Menu item	Assignment			
Embedded NAND Flash	Operation of sold	lered ATA Flash Disk controller is permitted (FLASH-disk)		
	[Enabled]	operation is permitted		
	[Disabled]	operation if prohibited		
Reserve BIOS Switch by	Control of switch	ing to BIOS backup copy		
WDT	[Enabled]	function of switching to BIOS backup copy is activated (in case of hang-up, during completion of the POST procedure)		
	[Disabled]	function of switching to BIOS backup copy is deactivated (in case of hang-up, during completion of the POST procedure), the function is deactivated immediately after th start of BIOS		
Start Manufacturing Link	nk       Activating the mode of direct access to Primary IDE Master via a consol port.         It contains information on CPU manufacturer, as well as items to control o of integrated Cache-memory of CPU			
CPU Configuration (submenu)				
IDE Configuration         Operation control of devices on IDE bus           (submenu)         Operation control of devices on IDE bus				
Remote Access Configuration	Console input-output settings			

Menu item	Assignment
(submenu)	
USB Configuration (submenu)	Settings of USB ports. These settings apply to all 4 USB ports.

## 5.2.1 CPU Configuration

Screen of "CPU Configuration" menu is shown in Figure 5.5, description of items is given in the table 5.3.

	BIOS SETUP UTILITY				
	Advanced				
* 1	***************************************	***	* * * * *	*****	***
*	CPU Configuration	*		Options	*
*	Module Version - 00.01	*			*
*	***************************************	* *	Disa	bled	*
*	Manufacturer: RDC	*	Enab	led	*
*	Brand String: Vortex86DX A9121	*			*
*	Frequency : 600MHz	*			*
*		*			*
*	L1 Cache [Enabled]	*			*
*	Cache L1 : 16 KB	*			*
*	L2 Cache [Enabled]	*			*
*	Cache L2 : 256 KB	*			*
*		*			*
*		*	*	Select Screen	*
*		*	**	Select Item	*
*		*	+-	Change Option	*
*		*	F1	General Help	*
*		*	F 6	Reset WDT	*
*		*	F10	Save and Exit	*
*		*	ESC	Exit	*
*		*			*
* 1	* * * * * * * * * * * * * * * * * * * *	***	* * * * *	****	* * *
	vO2.61 (C)Copyright 1985-2006, American N	leq	atren	ds, Inc.	

Fig. 5-5: Screen of "CPU Configuration" menu

 Table 5-3:
 Description of "CPU Configuration" menu

Menu item	Assignment		
L1 Cache	[Enabled]	Operation of L1 Cache-memory is permitted	
	[Disabled]	Operation of L1 Cache-memory is prohibited	
L2 Cache	[Enabled]	Operation of L2 Cache-memory is permitted	
	[Disabled]	Operation of L2 Cache-memory is prohibited	

## 5.2.2 IDE Configuration

Screen of "IDE Configuration" menu is shown in figure 5.6, description of items is given in the table 5.4.

B Advanced	IOS SETUP UTILITY		
******	* * * * * * * * * * * * * * * * * * * *	* * *	* * * * * * * * * * * * * * * * * * * *
* IDE Configuration * ******************************	* * * * * * * * * * * * * * * * * * * *		DISABLED: disables the * integrated IDE *
* OnBoard PCI IDE Controller	[Primary]		Controller. 7
* OnBoard IDE Operate Mode *	[Legacy Mode]		PRIMARY: enables only 7 the Primary IDE 7
* * Primary IDE Master * * Primary IDE Slave *	: [Not Detected] : [Hard Disk]	* *	Controller.
	[Disabled] [35] [Host & Device]	* *	
* * *			* Select Screen * ** Select Item *
* * *		*	+- Change Option 7 F1 General Help 7 F6 Reset WDT 7
* *		*	F10 Save and Exit * ESC Exit *
* ************************************	**************************************	* * * *	* ************************************



 Table 5-4:
 Description of "IDE Configuration" menu (IDE controller configuration)

Menu item	Assignment			
Onboard PCI IDE	Operation control	of integrated PCI controller of IDE bus.		
Controller	[Primary] operation is permitted			
	[Disabled]	operation if prohibited		
Primary IDE Master (submenu)	It contains inform (Fig 5.5, table 5.3	ation on the connected IDE device, operating in the Master mode 3).		
Primary IDE Slave (submenu)	It contains information on the connected IDE device, operating in the Master mode. Menu structure is gully identical to the Primary IDE Master menu structure (Fig. 5.5, table 5.3).			
Hard Disk Write Protect	Permission to set the access lockout for writing to IDE devices			
	[Enabled] Set the lockout			
	[Disabled]	lift the lockout		
IDE Detect Time Out (Sec)	Waiting limit for determination of ATA/ATAPI device, in seconds. The following values are available:			
	[0], [5], [10], [15],	[20], [25], [30] , <u>[35]</u>		
ATA(PI) 80Pin Cable	Selection of a wa	y for determination of 80-wire ATA(PI) cable		
Detection	[Host & Device]	check from the side of system and IDE devices		
	[Host]	check only from the side of system		
	[Device]	check only from the side of IDE devices		

#### 5.2.2.1 Primary IDE Master (Configuration of IDE Primary Master)

Screen "Primary IDE Master" menu is shown in the figure 5.7, description of items is given in the table 5.5. "IDE Primary Slave" menu is fully identical to the "Primary IDE Master" menu.

BIOS SETUP UTILITY				
Advanced	*****	**	* * * *	*****
* Primary IDE Slave				ect the type *
* **********************	****			
* Device :Hard Disk				the system.
* Vendor : Fastwel Embedded AT	d Floch Dieb	*		the system.
* Size :OMB	A FIASH DISK	÷.		
		÷		
* LBA Mode :Supported		÷.		
* Block Mode:Not Supported		÷.		
* PIO Mode :4				
* Async DMA :MultiWord DMA-2				
* Ultra DMA :Ultra DMA-2 *				7
* S.M.A.R.T.:Supported		*		7
* ***********************	* * * * * * * * * * * * * * * * * * * *	*		7
* Type	[Auto]	*	*	Select Screen *
* LBA/Large Mode	[Auto]	*	**	Select Item *
* Block (Multi-Sector Transfer)	[Auto]	*	+-	Change Option *
* PIO Mode	[Auto]	*	F1	General Help *
* DMA Mode	[Auto]	*	F 6	Reset WDT *
* S.M.A.R.T.	[Auto]	*	F10	Save and Exit *
* 32Bit Data Transfer	[Enabled]	*	ESC	Exit *
*		*		*
********	* * * * * * * * * * * * * * * * * * * *	**	* * * *	*****
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Fig. 5-7:	Screen "Primary IDE Master" menu
-----------	----------------------------------

 Table 5-5:
 Description of "Primary IDE Master" menu

Menu item	Assignment		
Туре	Type of device co	nnected to this IDE channel	
	[Not Installed]	Prohibition for searching for the connected devices	
	[Auto]	Automatic detection of connected device type	
	[CD/DVD]	Determine the connected device as CD/DVD drive	
	[ARMD]	Determine the connected device as ATAPI removable data storage device (ZIP, LS-120)	
LBA/Large Mode	Addressing type of	of device connected to this IDE channel	
	[Auto]	Automatic determination of LBA mode support	
	[Disabled]	Prohibition of LBA mode determination, Large Mode is used	
Block (Multi-Sector	Mode of block dat	ta transmission	
Transfer)	[Auto]	This option enables BIOS to automatically determine, whether the Multi-Sector Transfers mode is supported on this channel. This option enables BIOS to automatically determine the number of sectors per block for transmission from the hard drive to memory. Data to/from the device will be transmitted via several sectors per unit of time. Default value.	
	[Disabled]	This option prohibits BIOS to use the Multi–Sector Transfer mode on this channel. Data to/from the device will be transmitted via a single sector per unit of time.	

Menu item	Assignment			
PIO Mode	Programmable input-output (PIO) mode			
	[Auto]	his option enables BIOS to automatically determine whether a device supports the PIO mode. It is recommended to use this unit when it is impossible to determine which mode is supported by the connected device		
	[0], [1], [2], [3], [4]	St the PIO 0,1,2,3,4 mode for the connected device.		
		Data transmission rate in the mode		
		PIO 0 – up to 3.3 MB/sec,		
		PIO 1 – up to 5.2 MB/sec,		
		PIO 2 – up to 8.3 MB/sec,		
		PIO 3 – up to 11.1 MB/sec,		
		PIO 4 – up to 16.6 MB/sec.		
DMA Mode	DMA (Direct Memo	bry Access) mode of data transmission		
	[Auto]	Recommended value for the most efficient data transmission. BIOS will automatically determine the most relevant DMA mode.		
	[SWDMA0] [SWDMA1] [SWDMA2]	"Single Word DMA" modes		
	[MWDMA0] [MWDMA1] [MWDMA2]	"Multi Word DMA" modes		
S.M.A.R.T.	Smart Monitoring,	Analysis, and Reporting Technology		
	[Auto]	BIOS will automatically determine and support the connected device. It is recommended to use this option when it is impossible to determine and support of the connected drive.		
	[Enabled]	This option enables BIOS to use the SMART function during operation with the connected drives		
	[Disabled]	This option prohibits BIOS to use the SMART function during operation with the connected drives		
32-bit Data Transfer	32-bit Data Transfe	er Mode		
	[Enabled]	This option enables to use 32 bit data transmission for the device connected		
	[Disabled]	This option prohibits to use the 32 bit data transmission for the device connected		

\* Available volume of integrated drive – 1.8 GB (incorrect determination of the volume of integrated drive is attributed to peculiarities of AMI BIOS operation).

#### 5.2.3 Remote Access Configuration

Screen of "Remote Access Configuration" menu is shown in the Figure 5.8, description of items is given in the table 5.6.

	B	IOS SETUP UTILITY				
	Advanced					
* 1	* * * * * * * * * * * * * * * * * * * *	*****	* * 1	* * * * * * *	*****	****
*	Configure Remote Access type a				Remote Access	*
*	* * * * * * * * * * * * * * * * * * * *	******	*	type.		*
*	Remote Access	[Enabled]	*			*
*			*			*
*	Serial port number	[COM3]	*			*
*	Base Address, IRQ	[3F8h, 4]	*			*
*	Serial Port Mode	[115200 8,n,1]	*			*
*	Flow Control	[None]	*			*
*	Redirection After BIOS POST	[Boot Loader]	*			*
*	Terminal Type	[ANSI]	*			*
*	VT-UTF8 Combo Key Support	[Disabled]	*			*
*	Sredir Memory Display Delay	[No Delay]	*			*
*	Terminal Display Mode	[Recorder Mode]	*	* 8	Select Screen	*
*	Terminal Size	[80 X 25]	*	* *	Select Item 👘	*
*	*******	* * * * * * * * * * * * * * * * * * * *	*	+-	Change Option	*
*	Manufacturing Link Mode	[Disabled]	*	F1	General Help	*
*			*	F 6	Reset WDT	*
*			*	F10	Save and Exit	*
*			*	ESC	Exit	*
*			*			*
* 1	* * * * * * * * * * * * * * * * * * * *	* * * * * * * * * * * * * * * * * * * *	* * :	* * * * * * *	*****	****
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Fig.	5_9.	Screen of "Remote Access Configuration" r	monu
FIY.	J-0.	Screen of Remote Access Configuration	nenu



#### Attention!

Console I/O module integrated into BIOS carries out scanning of the available COM-ports during system start. Scanning is carried out using base addresses in the following sequence: 0x3F8, 0x2F8, 0x3E8, 0x2E8. In BIOS Setup "Advanced -> Remote Access Configuration" section, the first available port obtains the number of COM1 and further in the right order. If the number of available COM-ports changes during the next start of the system (e.g. by changing the settings of "SouthBridge Configuration -> Serial/Parallel Port Configuration"), in this case it can result in a displacement of actual base address and COM-port, used for console I/O.

E.g. if COM3 has been selected as a console port, and then COM 1 has been deactivated in the "South Bridge Configuration" settings and other parameters remained as by default, in this case after system restart there will be displacement of the console COM-port by 1, in such a way that for console I/O COM 4 parameters will be used (the third in succession among the available COM-ports).

#### Table 5-6: "Remote Access Configuration" menu description (Console I/O settings)

Menu item	Assignment			
Remote Access	Console I/O	Console I/O		
	[Disabled]	Console I/O is deactivated		

Menu item	Assignment		
	[Enabled]	Console I/O is activated, additional options of console I/O parameters setting become available.	
Serial port number	Selection of console I/O serial port		
	[COM1]	COM1 port is used as console I/O port	
	[COM2]	COM2 port is used as console I/O port	
	[COM3]	COM3 port is used as console I/O port	
	[COM4]	COM4 port is used as a console I/O port	
Serial port mode	Operation mode o	f the console I/O port	
	[ <u>115200 8,n,1]</u> ,	Data transmission speed115,2 kbaud, 8 bit, without parity check, 1 stop bit	
	[57600 8,n,1],	Data transmission speed 57,6 kbaud, 8 bit, without parity check, 1 stop bit	
	[38400 8,n,1],	Data transmission speed 38,4 kbaud, 8 bit, without parity check, 1 stop bit	
	[19200 8,n,1],	Data transmission speed 19,2 kbaud, 8 bit, without parity check, 1 stop bit	
	[09600 8,n,1],	Data transmission speed 9,6 kbaud, 8 bit, without parity check, 1 stop bit	
Flow Control	Control of symbol	stream for console port	
	[None]	No	
	[Hardware]	CTS/RTS hardware control	
	[Software]	XON/XOFF software control	
Redirection After BIOS	Console I/O opera	tion mode after the POST procedure of by BIOS	
POST	[Disabled]	Disable the console I/O after the POST procedure by BIOS	
	[Boot Loader]	Console I/O is active during the POST procedure by BIOS and during OS booting	
	[Always]	Console I/O operates constantly. Certain OS could not work in case this option is selected.	
Terminal Type			
	[ANSI]	ANSI standard	
	[VT100]	VT100 standard	
	[VT-UTF8]	VT-UTF8 standard	
VT-UTF8 Combo Key	Support of VT-UT	F8 symbols for ANSI/ME100 terminals	
Support	[Disabled]	Support is deactivated	
	[Enabled]	Support is allowed	
Sredir Memory Display Delay	Delay of module installed RAM to c	booting during displaying the screen with information on the console PC	
	[No Delay]	Without delay	
	[Delay 1 Sec],	Set the delay for 1 sec.	
	[Delay 2 Sec],	Set the delay for 2 sec.	
	[Delay 4 Sec]	Set the delay for 4 sec.	
Terminal Display Mode	Mode of data transmission to console PC		
	[Normal Mode]		
	[Recorder Mode]	Only text	

Menu item	Assignment		
Terminal Size	Number of transferred symbols and lines		
	[80x24]	80 symbols, 24 lines	
	[80x25] 80 symbols, 25 lines		
Manufacturing Link Mode	"Manufacturing Link" mode. Enables to gain access to the connected data sto media using the special-purpose software via COM-port, selected.		
	[Disabled]	Support is deactivated	
	[Enabled]	Support is allowed	

# 5.2.4 USB Configuration

Screen of "USB Configuration" menu is shown in Figure 5.9, description of the items is given in the Table 5.7.

Advanced	* * * * * * * * * * * * * * * * * * * *	* * *		* * * * * * * * * * * * * * * * * * *
USB Configuration				les support for
****	****	*		ev USB. AUTO
Module Version - 2.24.2-13.4		*		on disables
		*	legad	cy support if
USB Devices Enabled :				3B devices are
1 Keyboard, 1 Mouse, 1 Hub		*	conne	ected.
		*		
Legacy USB Support	[Enabled]	*		
USB 2.0 Controller Mode	[HiSpeed]	*		
BIOS EHCI Hand-Off	[Enabled]	*		
		*		
		*		
			*	Select Screen
			**	Select Item
			+-	
			F1	
				Reset WDT
				Save and Exit
		*	ESC	Exit
	*****			

Fig. 5-9: Screen of "USB Configuration" menu

Table 5-7: Description of "USB Configuration	n" menu (Configuration of USB ports)
--	--------------------------------------

Menu item	Assignment						
Legacy USB Support	Support of Legac	Support of Legacy USB mode.					
	[Disabled]	Disabled] Legacy USB mode is deactivated					
	[Enabled]	habled] Legacy USB mode is activated					
	[Auto]	Legacy USB mode is activated only if at least one USB device is connected					

Menu item	Assignment					
USB 2.0 Controller	Determination of	Determination of the speed of data exchange with USB device				
Mode	[HiSpeed]	data exchange speed is 25-480 Mb/sec				
	[FullSpeed]	[FullSpeed] data exchange speed is 0,5-12 Mb/sec (USB 1.0/1.1 mode)				
USB EHCI Hand-Off	Mechanism of interface control transfer EHCI (Enhanced Host Controlle between devices, with support of BIOS resources					
	[Disabled]	controlled by operating system				
	[Enabled]	controlled by BIOS resources				

In case of detection of a USB drive (USB Mass Storage Device Configuration), an additional submenu is available. Screen of the "USB Mass Storage Device Configuration" menu is shown in the Figure 5.10, description of items is given in the Table 5.8.



BIOS SETUP UTILITY Advanced		
**************************************	*****	* * *
* USB Mass Storage Device Configuration	* Number of seconds	*
* *********	* POST waits for the	*
* USB Mass Storage Reset Delay [20 Sec]	* USB mass storage	*
*	* device after start	*
* Device #1 UFD Silicon-Power4G 1100	* unit command.	*
* Emulation Type [Auto]	*	*
*	*	*
*	*	*
*	*	*
*	*	*
*	*	*
*	*	*
*	* * Select Screen	*
*	* ** Select Item	*
*	* +- Change Option	*
*	* F1 General Help	*
*	* F6 Reset WDT	*
*	* F10 Save and Exit	*
*	* ESC Exit	*
*	*	*
* * * * * * * * * * * * * * * * * * * *	* * * * * * * * * * * * * * * * * * * *	* * *
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 Table 5-8:
 Description of "USB Mass Storage Device Configuration" menu (Configuration of USB drive)

Menu item		Assignment					
Emulation Type	Operation mode.						
	[Auto]	Automatic mode					
	[Floppy]	Emulation type of the drive on floppy disks					
	[Forced FDD]	Forced emulation mode of the drive on floppy disks					
	[Hard Disk]	HDD emulation mode					
	[CDROM]	CDROM emulation mode					

# 5.3 PCI/ PnP (additional settings of PCI plug and play)

This tab contains items responsible for operation of PCI and ISA buses, as well as control of interrupt switching. Screen of "PCI/ PnP" menu is shown in Figures 5.11 and 5.12, description of the menu is given in the Table 5.9.

	BIOS SETUP UTILITY								
Main	Advanced	PCIPnP	Boot	Security	Chi	pset	Exit		
******	* * * * * * * * * * * *	* * * * * * * * * * *	******	* * * * * * * * * * *	*****	****	*****	****	
* Advanc	ed PCI/PnP S	ettings			**	Clea	r NVRAM during 👘	1	
* *****	********	*******	*******	* * * * * * * * * * *	*****	Syst	em Boot.	1	
* WARNIN	G: Setting w	rong value:	s in belo	ow sections	**			1	
*	may cause	system to	malfunct	cion.	**			1	
*					**				
* Clear	NVRAM		[No]		* *				
* Plug &	Play O/S		[No]		**			1	
* PCI La	tency Timer		[64]		**			1	
* Alloca	te IRQ to PC	I VGA	[No]		**			1	
* Palett	e Snooping		[Disal	oled]	**				
* PCI ID	E BusMaster		[Enab.	led]	**			1	
* OffBoa	rd PCI/ISA I	DE Card	[Auto]		**				
*					**	*	Select Screen	1	
* IRQ3			[Resei	rved]	* *	**	Select Item	7	
* IRQ4			[Resei	rved]	* *	+-	Change Option	3	
* IRQ5			[Avai]	lable]	* *	F 1	General Help		
* IRQ7			[Avai.	lable]	* *	F 6	Reset WDT	1	
* IRQ9			[Avai]	lable]	* *	F10	Save and Exit		
* IRQ10			[Avai.	lable]	* *	ESC	Exit	1	
* IRQ11			[Resei	rved]	**			1	
******	* * * * * * * * * * * *	* * * * * * * * * *	******	* * * * * * * * * * *	*****	* * * * *	* * * * * * * * * * * * * * * * * * *	***	
	v02.61 (	C)Copyright	t 1985-20	006, Americ	an Meq	atren	ds, Inc.		

#### Fig. 5-11: Screen of "PCI/ PnP" menu

Main Ad	vanced	PCIPnP	Boot	Security	Chij	pset	Exit	
********	* * * * * * * * *	******	******	******	* * * * * * *	* * * * * *	******	****
* Palette Sn	ooping		[Disak	led]	**	Avail	lable: Specified	*
* PCI IDE Bu	sMaster		[Enabl	.ed]	* *	IRQ i	is available to	be *
* OffBoard P	CI/ISA 1	DE Card	[Auto]		* *	used	by PCI/PnP	*
*					* *	devic	es.	*
* IRQ3			[Reser	ved]	* *	Reser	ved: Specified	*
* IRQ4			[Reser	ved]	* *	IRQ i	is reserved for	*
* IRQ5			[Avai]	able]	**	use b	y Legacy ISA 👘	*
* IRQ6			*** Opt	ions *:	** **	devic	es.	*
* IRQ7			* Availabl	.e	* **			*
* IRQ9			* Reserved	l I	* **			*
* IRQ10			* From ISA	_IRQ3	* **			*
* IRQ11			* From ISA	IRQ7	* **			*
* IRQ14			* * * * * * * * * *	*****	* *	*	Select Screen	*
* IRQ15			[Avai]	.able]	**	**	Select Item	*
*					**	+-	Change Option	*
* DMA Channe	10		[Avai]	able]	**	F1	General Help	*
* DMA Channe	1 1		[Avai]	able]	* *	F 6	Reset WDT	*
* DMA Channe	1 3		[Avai]	able]	* *	F10	Save and Exit	*
* DMA Channe	15		[Avai]	.able]	* *	ESC	Exit	*
* DMA Channe	16		[Avai]	able]	**			*
* * * * * * * * * * * *	* * * * * * * * *	*******	******	*****	* * * * * *	* * * * * *	* * * * * * * * * * * * * * * *	* * * *

Fig. 5-12:	Screen of "PCI/ PnP" menu (continued)
------------	---------------------------------------

Table 5-9:

Description of "PCI/ PnP" menu (additional settings of PCI Plug and Play)

Menu item	Assignment					
Clear NVRAM	Reset of the table of	of PnP parameters				
	[ <u>No</u> ]	Without change				
	[Yes]	Reset table after reboot				
Plug & Play O/S	OS with PnP suppo	ort is installed				
	[ <u>No</u> ]	No				
	[Yes]	Yes				
PCI Latency Timer		of PCI bus strokes, during which the device connected to the cupied, transmitting data.				
	[32], [ <u>64</u> ], [96], [128	3], [160], [192], [224], [248]				
Allocate IRQ to PCI VGA	Permission of interrupt purpose to the graphics card on PCI bus					
	[ <u>No</u> ]	Not to assign interrupt to the PCI graphics card				
	[Yes]	Assign interrupt to the PCI graphics card				
Palette Snooping	Synchronization of card (video editing	f graphics card palette and image, video captured with the I/O card).				
	[Disabled]	Function is deactivated Recommended value				
	[Enabled]	Function is activated				
PCI IDE BusMaster	Permission for usin	g the Bus Mustering PCI mode by the IDE bus controller				
	[Disabled]	Prohibit the use of Bus Mastering mode				
	[Enabled]	Permit the use of Bus Mastering mode				
OffBoard PCI/ISA IDE	Selection of the ext	ternal PCI/ISA card of IDE bus controller				
Card	[Auto]	Automatic detection of presence of the PCI/ISA card of IDE bus controller. Recommended value.				

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Menu item		Assignment			
	[PCI Slot1], [PCI Slot2], [PCI Slot3], [PCI Slot4], [PCI Slot5], [PCI Slot6]	Specify that the relevant PCI slot contains the installed IDE bus controller card			
IRQ3	Redundancy of IRQ	interrupt for internal Legacy devices SNK Vortex86DX			
IRQ4 IRQ5	[Available]	Permit the use of this interrupt for external PCI/PnP devices			
IRQ6 IRQ7	[Reserved]	Prohibit the use of this interrupt for external PCI/PnP devices, reserve for Legacy device.			
IRQ9 IRQ10 IRQ11 IRQ12 IRQ14 IRQ15	[From ISA_IRQx]	Use interrupt redirection. E.g., option [From ISA_IRQ3], installed for IRQ10 interrupt means redirection of IRQ3 interrupt line of ISA bus to the IRQ10 line of ISA bus controller of Vortex86DX CPU.			
	[SYSTEM_EVENT]	Use of the interrupt line for indication of SYSTEM_EVENT (see <u>Section 2.8.4</u> "Register of control / state of system interrupts")			
DMA Channel 0	Redundancy of DMA channel for internal Legacy devices SnK Vortex86DX				
DMA Channel 1 DMA Channel 3 DMA Channel 5	[Available]	Permit the use of this DMA channel to external PCI/PnP devices			
DMA Channel 5 DMA Channel 6 DMA Channel 7	[Reserved]	Prohibit the use of this DMA channel to external PCI/PnP devices, reserve for Legacy devices			
Reserved Memory Size	BIOS reservation of memory for devices based on ISA bus				
	[Disabled]	Prohibit reservation of memory for ISA devices on ISA bus by BIOS. Recommended value.			
	[16k], [32k], [64k]	Reserve the specified volume of memory for devices based on ISA bus			
SYSTEM_EVENT	[EXT_INT]	Only external interrupt source (XP17, XP18) participates in generation of SYSTEM_EVENT.			
	[PWR_FAIL]	Only the Power_Fail event from power supply supervisor (reduction of input power supply lower than the level of 4.65V) participates in generation of SYSTEM_EVENT.			
	[WDT2]	Only event of a watchdog timer, integrated into the power supply supervisor, participates in generation of SYSTEM_EVENT.			
	[EXT_INT& PWR_FAIL]	Generation of SYSTEM_EVENT is carried out with participation of [EXT_INT] and [PWR_FAIL] events (via "or").			
	[ALL]	Generation of SYSTEM_EVENT is carried out with participation of [EXT_INT] and [PWR_FAIL] and [WDT2] events (via "or").			

# 5.4 Boot (Boot modes)

This tab contains items, responsible for module booting modes as well as for choosing the IDE device which will be used for booting operating system. Screen of "Boot" menu is shown in the Figure 5.13, description of the items is given in the Table 5.10.



	BIOS SETUP UTILITY									
Main	Advanced	PCIPnP	Boot	Security	Chi	pset	Exit			
*****	******	*******	*****	* * * * * * * * * * * * * *	****	*****	******	* * * * *		
* Boot	Settings				*	Confi	gure Settings	*		
* ****	*****	******	*****	* * * * * * * * * * * * * *	** *	durin	g System Boot.	*		
* * Boo	ot Settings Co	nfiguration			*			*		
*					*			*		
* 1st	Boot Device		[HDD:]	PS-SanDisk SD	C] *			*		
*					*			*		
*					*			*		
*					*			*		
*										
* +								1		
<u>_</u>						*	Calast Courses	1		
+						**	Select Screen Select Item			
*					*		Go to Sub Scr	oon t		
*					*		General Help	* 199		
*					*		Reset WDT	*		
*					*			*		
*						ESC		*		
*					*	200	2	*		
*****	*****	*******	*****	* * * * * * * * * * * * *	****	*****	*****	* * * * *		
	v02.61 (	C)Copyright	1985-20	006, American	Med	atrend	s, Inc.			

#### Table 5-10: Description of the "Boot" menu (boot modes)

Menu item	Assignment
Boot Settings Configuration (submenu)	
<b>1st Boot Device</b> <b>Priority</b> (submenu)	

## 5.4.1 Boot Settings Configuration

Screen of the "Boot Settings Configuration" menu is shown in the Figure 5.14, description of menu items is given in the Table 5.11.

	BIOS SETUP UTILITY Boot				
******	* * * * * * * * * * * * * * * * * * * *	***	* * * * *	* * * * * * * * * * * * * * * * * *	**
Boot Settings Configuration		*	A110	ws BIOS to skip	
******	* * * * * * * * * * * * * * * * * * * *	*	cert	ain tests while 👘	
Quick Boot	[Enabled]	*	boot	ing. This will	
AddOn ROM Display Mode	[Force BIOS]	*	decr	ease the time	
Bootup Num-Lock	[On]	*	need	ed to boot the 👘	
PS/2 Mouse Support	[Auto]	*	syst	em.	
Wait For 'F1' If Error	[Enabled]	*			
Hit 'DEL' Message Display	[Enabled]	*			
Interrupt 19 Capture	[Disabled]	*			
Support TFT console	[Enabled]	*			
		*			
		*			
		*	*	Select Screen	
		*	**	Select Item	
		*	+-	Change Option	
		*	F1	General Help	
		*	F6 👘	Reset WDT	
		*	F10	Save and Exit	
		*	ESC	Exit	
		*			
* * * * * * * * * * * * * * * * * * * *	* * * * * * * * * * * * * * * * * * * *	* * *	* * * * *	******	**

 Table
 5-11:
 Description of the "Boot Settings Configuration" menu

Menu item		Assignment		
Quick Boot				
	[Disabled]	Selection of this value ensures the complete self-testing of the system during power on		
	[Enabled]	Selection of this value enables to reduce the number of tests during the power on and this way to speed up the booting process		
Add On ROM Display				
Mode	[Force BIOS]	This value permits to output data to monitor from BIOS extension cards during the system booting		
	[Keep Current]	This value enables computer system to display only P.O.S.T. information during the booting process		
Bootup Num-Lock				
	[Off]	Bootup Num-Lock is OFF		
	[ <u>On</u> ]	Bootup Num-Lock is ON		
PS/2 Mouse Support				
	[Disabled]	Support is deactivated		
	[Enabled]	Support is activated		
	[Auto]	Automatic support detection Recommended value		
Wait for 'F1' If Error	Waiting for "F1"	Waiting for "F1" button pressing in case of an error		

Menu item	Assignment		
	[Disabled]	This option does not require waiting for user's interference in case of an error. This value should be selected only if you know the reason why the BIOS error is occurred	
	[Enabled]	Permit BIOS system to wait for pressing the "F1" button in case of an error during booting	
Hit 'DEL' Message Display	Display of "Hit Del to enter Setup" message during memory initialization (press DEL button for entering the setup program)		
	[Disabled]	Output of message is prohibited	
	[Enabled]	Output of message is permitted	
Interrupt 19 Capture	Interception of INT19 program interrupt		
	[Disabled]	BIOS prohibits additional controllers to intercept INT19 interrupt	
	[Enabled]	BIOS permits additional controllers to intercept INT19 interrupt	
Support TFT Console	Showing information on TFT-display in text mode after the OS control transfer		
	[Disabled]	Showing information on TFT-display in text mode of OS control transfer is prohibited	
	[Enabled]	Showing information on TFT-display in text mode of OS control transfer is permitted	

# 5.5 Security

Screen of "Security" menu is shown in the Figure 5.15, description of menu items is given in the Table 5.12.

			BIOS SET	UP UTILITY				
	Main Advanced	PCIPnP	Boot	Security	Chips	set	Exit	
* 1	* * * * * * * * * * * * * * * * * * * *	*******	*******	*******	* * * * * * *	* * * * * * *	*******	*****
*	Security Settings				* 3	Instal.	l or Change	the *
*	****	*******	*******	*******	*** * ]	passwoi	rd.	*
*	Supervisor Passwor	d :Not Ins	talled		*			*
*	User Password	:Not Ins	talled		*			*
*					*			*
*	Change Supervisor	Password			*			*
*	Change User Passwo	rd			*			*
*					*			*
*	Boot Sector Virus	Protection	[Disab	led]	*			*
*					*			*
*					*			*
Ξ.								
Ĩ.,					*		elect Screen	Ĩ
<u>.</u>							Select Item	
Ĵ.						Enter (		
Ĵ.							General Help	
Ĵ.							Reset WDT	
÷.						F1O S ESC I	Save and Exi Swit	° د
*					*	Loc 1	EXIC	+
* *	* * * * * * * * * * * * * * * * * * *	******	******	*******	*****	*****	*****	*****
	**02_61_7	C) Contraigh	+ 1085-20	06, American		trenda	Inc	

Fig. 5-15:	Screen of "Security" menu

Table 5-12: Description of "Security" menu

Menu item		Assignment
Change Supervisor Password	Change of pass P.O.S.T. proced	word for system booting permission (request is output during the lure)
Change User Password	Change of pass BIOS Setup)	word for access to BIOS Setup (request at the time of entering
	Protection of bo	ot sector against viruses
	[Disabled]	Selection of this value deactivates boot sector protection against viruses
	[Enabled]	Selection of "Enabled" value includes protection of boot sector against viruses.
Boot Sector Virus		If any program (or virus) executes Disk Format command or tries to write into the boot sector on a hard drive, in this case there will be a warning on the display.
Protection		An attempt to address to the boot sector in case of activated protection, the following messages will appear:
		Boot Sector Write!
		Possible VIRUS: Continue (Y/N)?_
		The following messages will appear in case of any attempt to format any hard drive via BIOS INT 13 Hard disk drive Service:
		Format!!!
		Possible VIRUS: Continue (Y/N)?_

\* \* \* \* \* \* \* \* \* \* \* \* \* \* \* \*

#### 5.6 **Chipset (integrated devices)**

Screen of "Chipset" menu is shown in the Figure 5.16. Description of menu items is given in the table 5.13.

			BIOS SE	TUP UTILITY		
Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit
******	* * * * * * * * * * * *	******	******	*****	******	* * * * * * * * * * * * * * * * * * * *
Advance	ed Chipset S	ettings			* Opti	ons for SB
*****	* * * * * * * * * * * *	* * * * * * * * * *	******	******	*** *	
UARNIN(	G: Setting w	rong value	s in bel	ow sections	*	
	may cause	system to	malfunc	tion.	*	
					*	
* Sout	hBridge Conf	iguration			*	
* Onboa	ard Devices				*	
					*	
					*	
					*	
					*	
					*	
					* *	Select Screen
					* **	Select Item
					* Ente	r Go to Sub Screen
					* F1	General Help
					* F6	Reset WDT
					* F10	Save and Exit
					* ESC	Exit
					*	
******	******	******	******	*****	*******	* * * * * * * * * * * * * * * * * *



Menu item	Assignment
SouthBridge Configuration (submenu)	
Onboard Devices (submenu)	Configuration of integrated devices (audio and video controllers)

## 5.6.1 SouthBridge Configuration

Screen of "SouthBridge Configuration" menu is shown in the Figure 5.17, description of menu items is given in the Table 5.14.

* USB Port 2,3       [Enabled]       *         * USB IRQ:       [use IRQ 6]       *         * SB LAN       [Enabled]       *         * LAN IRQ:       [IRQ 10]       *         * MAC Address F4 6D 04 66 6A 4B       *       *         * ISA Configuration       *       *         * * Serial/Parallel Port Configuration       *       *         * * WatchDog Configuration       *       *		BIOS SETUP UTILITY		
South Bridge Chipset Configuration       * A9121 LAN Enable         USB Port 0,1       [Enabled]         USB Port 2,3       [Enabled]         USB IRQ:       [use IRQ 6]         SE LAN       [Enabled]         LAN IRQ:       [IRQ 10]         MAC Address F4 6D 04 66 6A 4B       *         * Serial/Parallel Port Configuration       *         * WatchDog Configuration       *         * NV SRAM Configuration       *         * NV SRAM Configuration       *         * F1       General Help         * F6       Reset WDT         * F10< Save and Exit			Chipset	
<pre>view in the interview interview</pre>	* * * * * * * * * * * * * * * * * * * *	*****	*************	******
* USB Port 0,1       [Enabled]       *       *         * USB Port 2,3       [Enabled]       *       *         * USB IRQ:       [use IRQ 6]       *       *         * USB IRQ:       [IRQ 10]       *       *         * LAN       [RQ:       [IRQ 10]       *       *         * LAN IRQ:       [IRQ 10]       *       *       *         * MAC Address F4 6D 04 66 6A 4B       *       *       *       *         * ISA Configuration       *       *       *       *         * Serial/Parallel Port Configuration       *       *       *         * WatchDog Configuration       *       *       *       *         * NV SRAM Configuration       *       *       *       *         * Tildement Help       *       *       *       *         * NV SRAM Configuration       *       *       *       *         * Tildement Help       *       *       *       * <t< th=""><th></th><th></th><th></th><th>dble *</th></t<>				dble *
* USB Port 2,3       [Enabled]       *         * USB IRQ:       [use IRQ 6]       *         * SB LAN       [Enabled]       *         * SB LAN       [IRQ 10]       *         * LAN IRQ:       [IRQ 10]       *         * MAC Address F4 6D 04 66 6A 4B       *       *         * ISA Configuration       *       *         * Serial/Parallel Port Configuration       *       *         * WatchDog Configuration       *       *         * MV SRAM Configuration       *       *         * NV SRAM Configuration       *       *         * NV SRAM Configuration       *       *         * Select Streen       *       *         * NV SRAM Configuration       *       *         * Select Item       *       *         * Tister Street Item       *       *         * Select Item       *       *         * Tister Street Item       *       *         * Tister Street Item       *       *         * Tister Street Item       *       *         * Select Item       *       *         * Select Item       *       *         * Select Item       *       *     <	* *********	******	*** * or Disable	*
* USB IRQ:       [use IRQ 6]       *         * SB LAN       [Enabled]       *         * LAN IRQ:       [IRQ 10]       *         * MAC Address F4 6D 04 66 6A 4B       *       *         * * ISA Configuration       *       *         * * Serial/Parallel Port Configuration       *       *         * WatchDog Configuration       *       *         * GPIO Configuration       *       *         * NV SRAM Configuration       * **       Select Screen         * NV SRAM Configuration       * **       Select Item         * NV SRAM Configuration       * **       Select Item         * The General Help       *       *         * F1       General Help       *         * F10       Save and Exit       *         * ESC       Exit       *	* USB Port 0,1	[Enabled]	*	*
* SB LAN       [Enabled]       *         * LAN IRQ:       [IRQ 10]       *         * MAC Address F4 6D 04 66 6A 4B       *       *         * MAC Address F4 6D 04 66 6A 4B       *       *         * ISA Configuration       *       *         * Serial/Parallel Port Configuration       *       *         * WatchDog Configuration       *       *         * GPIO Configuration       *       *         * NV SRAM Configuration       * **       Select Screen         * NV SRAM Configuration       * **       Select Item         * NV SRAM Configuration       * **       Select Item         * F1 General Help       *       *         * F1 General Help       *       *         * F10 Save and Exit       *         * ESC Exit       *	* USB Port 2,3	[Enabled]	*	*
<pre>* LAN IRQ: [IRQ 10] * * * * * * * * * * * * * * * * * * *</pre>	* USB IRQ:	[use IRQ 6]	*	*
<pre>* MAC Address F4 6D 04 66 6A 4B  * * * * ISA Configuration * * Serial/Parallel Port Configuration * * WatchDog Configuration * * GPIO Configuration * * Select Screen * * NV SRAM Configuration * * Select Item * * * * * * * * * * * * * * * * * * *</pre>	* SB LAN	[Enabled]	*	*
<ul> <li>* ISA Configuration</li> <li>* ISA Configuration</li> <li>* Serial/Parallel Port Configuration</li> <li>* WatchDog Configuration</li> <li>* GPIO Configuration</li> <li>* Select Screen</li> <li>* NV SRAM Configuration</li> <li>* ** Select Item</li> <li>* +- Change Option</li> <li>* F1 General Help</li> <li>* F6 Reset WDT</li> <li>* F10 Save and Exit</li> <li>* ESC Exit</li> </ul>	* LAN IRQ:	[IRQ 10]	*	*
<pre>* ISA Configuration * * * * Serial/Parallel Port Configuration * * * * * * * * * * * * * * * * * * *</pre>	* MAC Address F4 6D 04 66	6A 4B	*	*
<pre>* * Serial/Parallel Port Configuration * * WatchDog Configuration * * GPIO Configuration * * Select Screen * * NV SRAM Configuration * ** Select Item * +- Change Option * +- Change Option * F1 General Help * F6 Reset WDT * F6 Reset WDT * F10 Save and Exit * ESC Exit</pre>	*		*	*
<pre>* * WatchDog Configuration * * Select Screen * * GPIO Configuration * * Select Item * * NV SRAM Configuration * ** Select Item * * +- Change Option * * +- Change Option * * F1 General Help * * F6 Reset WDT * * F10 Save and Exit * * ESC Exit * *</pre>	* * ISA Configuration		*	*
* * GPIO Configuration * * Select Screen * * * NV SRAM Configuration * ** Select Item * * +- Change Option * * +- Change Option * * F1 General Help * * F6 Reset WDT * * F10 Save and Exit * * ESC Exit * *	* * Serial/Parallel Port C	Configuration	*	*
* * NV SRAM Configuration * * NV SRAM Configuration * +- Change Option * +- Change Option * F1 General Help * F6 Reset WDT * F10 Save and Exit * ESC Exit	* * WatchDog Configuration	1	*	*
*     *     *     Change Option     *       *     *     *     F1     General Help     *       *     *     *     F6     Reset WDT     *       *     *     *     F10     Save and Exit     *       *     *     *     ESC     Exit     *	* * GPIO Configuration		* * Select S	Creen *
* * F1 General Help * * * F6 Reset WDT * * * F10 Save and Exit * * * ESC Exit *	* * NV SRAM Configuration		* ** Select	Item *
* * F6 Reset WDT * * * F10 Save and Exit * * * ESC Exit *	*		* +- Change	Option *
* * F10 Save and Exit * * * ESC Exit *	*		* F1 General	. Help 🛛 *
* ESC Exit	*		* F6 Reset W	IDT *
	*		* F10 Save an	nd Exit 👘 *
* *	*		* ESC Exit	*
	ħ		*	*
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Table 5-14: Description of "SouthBridge Configuration" menu (SouthBridge Configuration)

Menu item		Assignment	
USB Port 0,1	Control of opera	tion of 0 and 1st USB port	
	[Enabled]	Permit operation of ports	
	[Disabled]	Prohibit operation of ports	
USB Port 2,3	Control of opera	tion of the 2nd and 3rd USB ports	
	[Enabled]	Permit operation of ports	
	[Disabled]	Prohibit operation of ports	
USB IRQ	Selection of interrupt line for USB controller		
SB LAN	Control of operation of integrated Ethernet controller (LAN)		
	[Enabled]	Permit controller operation	
	[Disabled]	Prohibit controller operation	
LAN IRQ	Selection of interrupt line for LAN controller		
MAC Address (information field)	MAC-address of integrated Ethernet controller (LAN)		
ISA Configuration (submenu)	This option enables to install timings for ISA bus – operations of I/O and memory access		

Menu item	Assignment
Serial/Parallel Port Configuration (submenu)	This option sets the address / mode/ interrupt for serial and parallel ports
WatchDog Configuration (submenu)	Control of operation of WDT0, WDT1 integrated watchdog timers

### 5.6.2 Onboard Devices

Screen of "Onboard Devices" menu is showm in the Figure 5.18, description of menu items is given in the Table 5.15.

****	*****		ipset *****
	****		• Options
SM718 Video IC	[Enabled]	*	*
CMI8738 Audio IC	[Enabled]	*	* Auto
Used IRQ:	[Auto]	*	
		*	
		*	• IRO 15
		*	-
	*** Options	* * * *	r .
	* Auto	* *	r .
	* IRQ 5	* *	r
	* IRQ 10	* *	r
	* IRQ 15	* *	r
	*********	* * * *	* * Select Screen
		*	* ** Select Item
		*	+- Change Option
		*	• F1 General Help
		*	F6 Reset WDT
		*	F10 Save and Exit
		*	* ESC Exit
		*	£

Fig. 5-18:	Screen of "Onboard Devices" menu
------------	----------------------------------



Menu item	Assignment		
SM718 Video IC	Configuration of integrated controller SM718		
	[Enabled]	Integrated video controller is activated	
	[Disabled]	Integrated video controller is deactivated	
CMI8738 IC	Configuration of integrated audio controller CMI8738		
	[Enabled]	Integrated audio controller is activated	
	[Disabled]	Integrated audio controller is deactivated	

Menu item		Assignment
Used IRQ	Auto IRQ 5 IRQ 10 IRQ 15	Selection of interrupt for Audio controller

## 5.6.2.1 ISA Configuration

Screen of "ISA Configuration" menu is shown in the Figure 5.19, description of menu items is given in the Table 5.16.

	BIOS SETUP U		
		Chips	et
* * * * * * * * * * * * * * * * * * * *		***********	*****
* ISA Clock	[8.3MHz]	*	Options *
* ISA 16bits I/O wait-state		*	7
* ISA 8bits I/O wait-state			.3MHz *
* ISA 16bits Memory wait-state		* 1	.6.6MHz *
* ISA 8bits Memory wait-state	[4 clock]	*	*
*		*	*
*		*	*
*		*	*
*		*	*
*		*	*
*		*	*
*		*	*
*		* *	Select Screen *
*		* *	* Select Item *
*		* +	Change Option *
*		* F	1 General Help *
*			6 Reset WDT *
*		* F	10 Save and Exit *
*			SC Exit *
*		*	*
*****	*****	*****	*****
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Fig. 5-19: Screen of "ISA Configuration" menu
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Table 5-16:	Description of "ISA Configuration" menu (ISA configuration)

Menu item	Assignment			
ISA Clock	Clock frequency ISA_SYSCLK (CLK, XS2 connector, B20 output)			
	[ <u>8.3MHz]</u>	Set the clock frequency of 8.3 MHz		
	[16.6MHz]	Set the clock frequency of 16.6 MHz		
ISA 16bits I/O wait-state	Duration of I/O wait-state cycle at 16 bit memory reference on ISA bus			
	[1 clock], [2 clock], [3 clock], [4 clock], [5 clock], [6 clock], [7 clock], [8 clock]			
ISA 8bits I/O wait-state	Duration of I/O wait-state cycle at 8 bit memory reference on ISA bus			
	[1 clock], [2 clock], [3 clock], [ <u>4 clock]</u> , [5 clock], [6 clock], [7 clock], [8 clock]			
ISA 16bits Memory wait- state	Duration of Merr	nory wait-state cycle at 16 bit memory reference on ISA bus		
	[0 clock], [ <u>1 cloc</u>	k], [2 clock], [3 clock], [4 clock], [5 clock], [6 clock], [7 clock]		

Menu item	Assignment
ISA 8bits Memory wait- state	Duration of Memory wait-state cycle at 8 bit memory reference on ISA bus
	[1 clock], [2 clock], [3 clock], [ <u>4 clock]</u> , [5 clock], [6 clock], [7 clock], [8 clock]

# 5.6.2.2 Serial/Parallel Port Configuration

Screen of "Serial/Parallel Port Configuration" menu is shown in the Figure 5.20, description of menu items is given in the Table 5.17.

	BIOS SETUP UTILITY		
****	* * * * * * * * * * * * * * * * * * * *	Chipset	* *
* SB Serial Port 1	[3E8]	* A9121 Internal UART	
* Serial Port IRO 1	[IRQ4]	* Serial Port	
* Serial Port Baud Rate	[115200 BPS]	*	
* Terminator 120 Ohm	[Enabled]	*	
* SB Serial Port 2	[2E8]	*	
* Serial Port IRQ 2	[IRQ3]	*	
* Serial Port Baud Rate	[115200 BPS]	*	
<ul> <li>Terminator 120 Ohm</li> </ul>	[Enabled]	*	
* SB Serial Port 3	[3F8]	*	
* Serial Port IRO 3	[IRQ4]	*	
* Serial Port Baud Rate	[115200 BPS]	*	
* SB Serial Port 4	[2F8]	*	
* Serial Port IRO 4	[IRQ3]	* * Select Screen	
* Serial Port Baud Rate	[115200 BPS]	* ** Select Item	
* SB Parallel Port Address	[278]	* +- Change Option	
* Parallel Port Mode	[EPP 1.7 AND SPP]	* F1 General Help	
* Parallel Port IRO	[IRQ5]	* F6 Reset WDT	
*	[11/20]	* F10 Save and Exit	
*		* ESC Exit	
*		*	
·· * * * * * * * * * * * * * * * * * * *	* * * * * * * * * * * * * * * * * * * *	*****	* *
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<b>F</b> ! <b>F</b> 00.		
Fig. 5-20:	Screen of "Serial/Parallel Port Configuration" n	nenu

 Table
 5-17:
 Description of "Serial/Parallel Port Configuration" menu

Menu item	Assignment		
SB Serial Port 1 SB Serial Port 2	This option sets the address for the relevant serial port (for each port individually)		
SB Serial Port 3	[Disabled]	Port operation is prohibited	
SB Serial Port 4	[3E8]	3E8h I/O base address assignment	
	[2E8]	2E8h I/O base address assignment	
	[3F8]	3F8h I/O base address assignment	
	[2F8]	2F8h I/O base address assignment	
Serial Port IRQ 1 Serial Port IRQ 2	This option assigns the interrupt line for the relevant serial port (for each port individually)		
Serial Port IRQ 3	[IRQ3]	IRQ3 interrupt line assignment	
Serial Port IRQ 4	[IRQ4]	IRQ4 interrupt line assignment	
	[IRQ9]	IRQ interrupt line assignment	

Menu item	Assignment		
	[IRQ10]	IRQ10 interrupt line assignment	
	[IRQ11]	IRQ11 interrupt line assignment	
Serial Port Baud Rate	This option sets the speed of data exchange for the relevant serial port (for each port individually)		
	[2400 BPS], [48 [115200 BPS]	00 BPS], [9600 BPS], [19200 BPS], [38400 BPS], [57600 BPS],	
SB Parallel Port Address	This option sets	the address for LPT1 parallel port	
	[Disabled]	Port operation is prohibited	
	[378]	378h I/O base address assignment	
	[278]	278h I/O base address assignment	
Parallel Port Mode	This option sets	the operation mode for LPT1 parallel port	
	[BPP]	Operation mode "Bi-directional Parallel Port" (BPP)	
		Data receive-transmit mode for parallel port	
	[EPP 1.9 AND SPP]	Operation mode compatible with EPP 1.9 and SPP modes	
	[ECP]	Operation mode "Enhanced Capabilities Port" (ECP)	
		ECP uses DMA protocol for reaching the speed of data transmission up to 2.5 Mb/sec. ECP ensures symmetrical, bidirectional data communication	
	[ECP AND EPP 1.9]	Operation mode compatible with ECP and EPP 1.9 modes	
	[SPP]	Operation mode "Standard Parallel Port" (SPP)	
	[EPP 1.7 AND SPP]	Operation mode compatible with EPP 1.7 and SPP modes.	
		Operation mode "Enhanced Parallel Port" (EPP) uses parallel port existing signals for asymmetrical bidirectional data communication from the main device	
	[ECP AND EPP 1.7]	Operation mode compatible with ECP and EPP 1.7 modes	
Parallel Port IRQ	This option assig	gns the interrupt line for LPT1 parallel port	
	[ <u>IRQ5]</u>	IRQ5 interrupt line assignment	
	[IRQ7]	IRQ7 interrupt line assignment	

### 5.6.2.3 WatchDog Configuration

Screen of "WatchDog Configuration" menu is shown in the Figure 5.21, description of menu items is given in the table 5.18.

****	****		pset *****	* * * * * * * * * * * * * * * * * * *
WatchDog O Function	[Disabled]	*		Options
WatchDog 1 Function	[Enabled]	*		
WatchDog 1 Signal Select	[IRQ6]	*	IRQ3	
Boot timeout	[64 Sec]	*	IRQ4	
		*	IRQ5	
		*	IRQ6	
		*	IRQ7	
		*	IRQ9	
		*	IRQ10	)
		*	IRQ1:	1
			IRQ12	2
		*		
			*	Select Screen
			**	Select Item
			+-	
		*		General Help
				Reset WDT
			F10	
		*	ESC	Exit
		*		

Fig. 5-21: Screen of "WatchDog Configuration" I	menu
---	------

 Table 5-18:
 Description of "WatchDog Configuration" menu

Menu item	Assignment		
WatchDog 0 Function WatchDog 1 Function	Control of operation of WDT0, WDT1 watchdog timers integrated into SnK Vortex86DX CPU		
	[Disabled]	Timer operation is prohibited	
	[Enabled]	Timer operation is permitted	
WatchDog 0 Signal Select WatchDog 1 Signal Select	This option enables to define an action which will be chosen upon completion of counting time of the relevant watchdog timer. It is possible to generate one of the interrupts, including a non-maskable interrupt, as well as generate the module reset signal		
	[IRQ3], [IRQ4], [IRQ5], [IRQ6], [IRQ7], [IRQ9], [IRQ10], [IRQ11], [IRQ12], [IRQ15], [INMI], [ <u>Reset]</u>		
WatchDog 0 Timer WatchDog 1 Timer	Setting the time counting interval of the relevant timer. Watchdog timer counts backward during operation. If the value of 64 seconds is set, it will count to 0 and then will generate the RESET, NMI or IRQ signal. If during the backward counting the timer obtains a restart signal, it interrupts the counting process and starts to count again, from 64		
[1 Sec], [2 Sec], [4 Sec], [4 [256 Sec], [512 Sec]		[4 Sec], [8 Sec], [16 Sec], [32 Sec], [ <u>64 Sec],</u> [128 Sec], Sec]	

### 5.6.2.4 GPIO Configuration

Screen of "GPIO Configuration" menu is shown in the Figure 5.22, description of menu items is given in the Table 5.19.

BIOS SET	TUP UTILITY
	Chipset
**************	* * * * * * * * * * * * * * * * * * * *
GPIO Configuration	* Options
***************	******
GPIO PORT2 7AH [30] FUNC [IIII]	* IIII
GPIO PORT2 7AH [30] DATA [0000]	* IIIO
	* IIOI
GPIO PORT2 7AH [74] FUNC [IIII]	* IIOO
GPIO PORT2 7AH [74] DATA [0000]	* IOII
	* IOIO
	* IOOI
	* I000
	* OIII
	*
	* * Select Screen
	* ** Select Item
	* +- Change Option
	* F1 General Help
	* F6 Reset WDT
	* F10 Save and Exit
	* ESC Exit
	*
* * * * * * * * * * * * * * * * * * * *	* * * * * * * * * * * * * * * * * * * *

Fig. 5-22: Screen of "GPIO Configuration" menu
--

 Table 5-19:
 Description of "GPIO Configuration" menu

Menu item	Assignment				
GPIO PORT2 7AH [30] FUNC	Configuration of the relevant line of GPIO PORT2 port , integrated into the SnK Vortex86DX CPU, as input or output.				
GPIO PORT2 7AH [74]	Setting bit to 'I' assigns this bit as input. Setting bit to 'O' assigns this bit as output.				
FUNC	<pre>[IIII], [III0], [II0I], [II00], [I0II], [I010], [I001], [I000], [0000]</pre>				
GPIO PORT2 7AH [30] DATA	Setting condition of the relevant line of GPIO PORT2 port, integrated into SnK Vortex86DX CPU.				
GPIO PORT2 7AH [74]	Setting bit to '1' assigns the relevant output to '1'. Setting bit to '0' assigns the relevant output to '0'.				
DATA	[1111], [1110], [1101], [1100], [1011], [1010], [1001], [1000], <u>[0000]</u>				

#### 5.6.2.5 NV SRAM Configuration

Screen of "NV SRAM Configuration" menu is shown in the Figure 5.23, description of menu items is given in the Table 5.20.

	BIOS SETUP UTILITY				
			pset		
**********	*****		*****	******	* * * *
* NV SRAM Configuration		*		Options	
					1
* NV SRAM Function	[READ/WRITE]		C8000		1
* NV SRAM Page Base Address	[C8000]		CC000		1
			D0000		
		*	D4000		
	operens		D8000		
π	* C8000		DC000		
*	* CC000	* *			*
*	* D0000	* *			*
*	* D4000	* *			*
*	* D8000	* *			*
*	* DCOOO	* *	*	Select Screen	*
*	* * * * * * * * * * * * * * * * * * * *	** *	**	Select Item	*
*		*	+-	Change Option	*
*		*	F1	General Help	*
*		*	F 6	Reset WDT	*
*		*	F10	Save and Exit	*
*		*	ESC	Exit	*
*		*			*
* * * * * * * * * * * * * * * * * * * *	*****	* * * * * *	* * * * * *	*****	* * * *
v02.61 (C)Copyric	ht 1985-2006, America	an Meg	atrend	s, Inc.	

Fig.	5-23:	Screen of "NV SRAM Configuration" r	menu

 Table 5-20:
 Description of "NV SRAM Configuration" menu

Menu item	Assignment			
NV SRAM Function	Setting the operation mode of nonvolatile RAM			
	[Disabled] Operation of NV SRAM is prohibited			
	[READ ONLY]	Setting "READ ONLY" mode		
	[READ/WRITE] Setting the " READ/WRITE" mode			
NV SRAM Page Base Address	Setting a base address for page access to the nonvolatile RAM 128KB (page size 16 KB)			
	<u>C8000</u>	Base address – C8000h		
	CC000	Base address – CC000h		
	D0000	Base address – D0000h		
	D4000	Base address – D4000h		
	D8000	Base address – D8000h		
	DC000	Base address – DC000h		

# 5.7 Exit

Screen of "Exit" menu is shown in the Figure 5.24. Description of menu items is given in the Table 5.21.







Menu item	Assignment
Save Changes and Exit	Save the settings in CMOS and FRAM memory, and exit the BIOS Setup program
Discard Changes and Exit	Discard changes in CMOS and FRAM memory and exit
Discard Changes	Discard changes made in settings without exiting the BIOS Setup program
Load Optimal Defaults	Load optimal (factory) default settings without exiting the BIOS Setup program

# **SECTION 6**

TRANSPORTATION, UNPACKING AND STORAGE

# 6. TRANSPORTATION, UNPACKING AND STORAGE

# 6.1 Transportation

The module must be transported in individual factory packages consisting of an individual antistatic bag and a cardboard box, in closed vehicles (in heated and airtight compartments of motor, railroad or airborne vehicles) under storage conditions 5 as per GOST 15150-69 or under storage conditions 3 during transportation by sea.

It is allowed to transport modules packed in individual antistatic bags in factory multipacks.

Packed modules must be transported pursuant to the cargo transportation rules applicable to this mode of transport.

During loading and unloading work and transportation, packed modules must not be exposed to jerks, falls, shocks and atmospheric precipitation. The stowage of packed modules in a vehicle must exclude their shifting.

# 6.2 Unpacking

The modules that were transported at subzero ambient temperature must be stored for 6 hours under storage conditions 1 as per GOST 15150-69 before they can be unpacked.

Placing packed modules in front of a heat source before their unpacking is forbidden.

In the process of the modules unpacking one must observe all the precautions ensuring their safety and marketable appearance of the factory packages.

Upon unpacking, the modules must be checked for external mechanical damage after transportation.

# 6.3 Storage

Modules storage conditions: 1 as per GOST 15150-69 (IEC721).

# **ANNEXES**

# ANNEXES

# A Tables of contacts for connecting displays

SGD-DEMO or EL240.128.45 connector		LPT connector (XP5, IDC2-26)	
1	VH (+12V)	-	
2	VH (+12V)	-	
3	GND	-	
4	GND	-	
5	VL (+5V)	26	+5V
6	RES	-	
7	/WR	1	STB*
8	/RD	6	INIT*
9	/CS	10	GND
10	AO	2	AFD*
11	SELFTEST	12	GND
12	GND	14	GND
13	D0	3	DATA0
14	D1	5	DATA1
15	D2	7	DATA2
16	D3	9	DATA3
17	D4	11	DATA4
18	D5	13	DATA5
19	D6	15	DATA6
20	D7	17	DATA7
21	SEL1	16	GND
22	READY	-	
23	GND	22	GND
24	LUMA	-	

Table A-1:

: Table of cable contact for connection of 4 bit STN EL-displays to LPT port

\* Connection of display to LPT port requires the development of a relevant driver

# B Frequently asked questions related to programming of CPC152

1. I need to use an external watchdog timer, however some functions of the library that I use, are performed longer than 1,6 seconds and as a result, the watchdog timer makes CPU to restart. I don't have the source texts of this library and as a consequence, can't insert a watchdog strobing procedure into the code. Microcontroller does not allow to repeatedly stop and restart the watchdog timer. What should I do?

Solution: If functions of your library operate at permitted interrupts, you should create your own program for pre-processing of occasionally emerging interrupts.

During the performance of library functions (at this time only!), you should strobe the watchdog timer in this pre-processor.

# 2. While working with CPC152, I use SmartLink terminal program. I noticed that some of the files transferred to the module using FTRANS.EXE program, are saved with errors. What could be the reason?

It happens because **SmartLink** program uses XMODEM protocol while exchanging files with **FTRANS.EXE** program. This protocol does not have a sufficient ability to detect transmission errors.

In order to completely exclude possibility of errors during file transmission, it is strongly recommended not to use **SmartLink**, and use the terminal program instead, which supports XMODEM/CRC (HYPERTERMINAL, TELEMAX, TERM90, TERM95) exchange protocol.

In this case, for exchange of files the CPC152 is required to have the **FTRANS.EXE program**, written in "Fastwel", which is supplied from the beginning of March of 2001 and can be obtained at <u>ftp://ftp.prosoft.ru/pub/Hardware/Fastwel/CPx/CPC152/</u>. While transferring the file to module, it is recommended to launch the **FTRANS program** with the key /CRC.

During transfer of files with **FTRANS** it is also recommended to specify an exact size of the transferred file.

# 3. Problem with a console via COM-port. It is possible to enter BIOS Setup settings, but when DOS is started, using keyboard via terminal is unsuccessful. What could be the reason?

The most probable cause for that is in BIOS Setup settings. A remote console integrated into the AMI BIOS by default is switched on until the time BIOS will pass control to the operating system. In order to activate console I/O integrated into the AMI BIOS, it is required to change BIOS Setup settings – in section "Advanced -> Remote Access Configuration" it is necessary to set the parameter "Redirection after BIOS POST" to "Always" (By default this parameter is set to "Boot Loader" at the time of delivery). However it should be considered that console implemented in the AMI BIOS uses system timer.

It is also possible to use FreeDOS resources (OS preinstalled by default), namely the **MODE** commands (changing parameters of I/O devices) and **CTTY** (changing a standard I/O device) in AUTOEXEC.BAT file:

```
MODE COMm[:] [BAUD[HARD]=b] [PARITY=p] [DATA=d] [STOP=s]
CTTY COMm
```

**COMm** – used COM-port (COM1, COM2, COM3, COM4). <u>Remember!</u> That in BIOS Setup settings, for COM3 port (RS-232) and COM4 (RS-232) port base addresses of COM1 (3F8h) and COM2 (2F8h) ports are assigned by default – therefore they are recognized by FreeDOS operating system as COM1 and COM2 ports. In order to use COM3 (RS-232) for console I/O, it is required to set the BAUD parameter as equal to COM1.

**BAUD** – code of exchange speed: 96 – 9600 kbit/s, 192 – 19200 kbit/s.

**BAUDHARD** – code of exchange speed: 96 – 9600 kbit/s, 192 – 19200 kbit/s, 384 – 38400 kbit/s, 1152 – 115200 kbit/s.

**PARITY** – even parity (Even, Odd, Mark, Space, None)

**DATA** – number of data bits (7, 8)

**STOP** – number of stop bits (1, 2)

Examples of entries in AUTOEXEC.BAT file:

MODE COM1 BAUDHARD=1152 PARITY=NONE DATA=8 STOP=1 CTTY COM1

MODE COM2 BAUD=96 PARITY=NONE DATA=8 STOP=1 CTTY COM2

However, it is required to consider certain limitations when operating with the console while FreeDOS operating system is started (preinstalled to the integrated FLASH-drive during delivery), namely: pressing of such buttons as "Backspace" and " $\leftarrow$ ", " $\rightarrow$ " is carried out improperly (though such problems were not detected during operation with MSDOS OS).

# C Terms, abbreviations and acronyms

Term	Meaning	
ACPI	Advanced Configuration and Power Interface	
AGP	Accelerated Graphics Port	
AGTL	Advanced Gunning Transceiver Logic	
BIOS	Basic Input-Output System	
CRT-display	Cathode Ray Tube Display	
DAC	Digital-Analog Converter	
DDR SDRAM	Double Data Rate Synchronous Dynamic Random Access Memory	
DMA	Direct Memory Access	
DMI	Direct Media Interface	
DVMT	Dynamic Video Memory Technology	
ECC	Error Correction Code	
EEPROM	Electrically Erasable Programmable Read-Only Memory	
EHCI	Enhanced Host Controller Interface (Universal Serial Bus specification)	
EIDE	Enhanced Integrated Drive Electronics	
EOS	Electrical Overstress	
ESD	Electrostatically Sensitive Device	
	Electrostatic Discharge	
FSB	Frequency System Bus	
FWH	Firmware Hub	
GMCH	Graphics and Memory Controller Hub	
I <sup>2</sup> C™	Inter Intergrated Circuit	
LCD	Liquid crystal display	
LPC	Low Pin Count	
LVDS	Low Voltage Differential Signal	
MDI	Media Dependent Interface	
PC	Personal Computer	

Term	Meaning
PIO	Programmed Input/Output
PLCC	Plastic Leaded Chip Carrier
PM	Peripheral Management Controller
POST	Power On Self Test
PSB	Processor System Bus
PWM output	Pulse-Width Modulation
RAMDAC	Random Access Memory Digital-to-Analog Converter
RTC	Real Time Clock
SMB	System Management Bus
SMBus	System Management Bus
SODIMM	Small Outline Dual In-Line Memory Module
SSD	Solid State Disk
TFT	Thin Film Transistor
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver-Transmitter
UHCI	Universal Host Controller Interface
USB	Universal Serial Bus
UTP	Unshielded Twisted Pair