CPB907

Mezzanine CPU Module COM Express® mini, Type 10

User Manual

Rev. 1.0
June 2015

The product described in this manual is compliant with all related CE standards.

Product Title: CPB907
Document name: CPB907 User Manual
Manual version: 0.1

Revision Record

Revision No.	Brief description of changes	Board index	Revision date
0.1	Initial version	CPB907	March 2013
1.00	Item version: 1.2 Sections1.2 "General information", 1.5 "Board block diagram ", 1.7 "Module versions" – there were changes related to the RAM volume for various module versions (DDR2 RAM volume for CPB907-03 version has been increased up to 1 GB). Section 1.4 "Module power supply" – changes regarding requirements to power supply parameters. Section 1.8 "Delivery checklist" has been added with information on cooling system options. Section 1.9 "Additional accessories" – order number for development kit has been changed (KIB1283-02). Section 2.1 "General technical specifications for CPB907" – changes related consumption current of various versions of CPB907 were made, added information on weight and dimensions of the module with the installed cooling system.	CPB907	September 2013

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TRANSPORTATION, UNPACKING AND STORAGE

Transportation

The device should be transported in original manufacturer's separate packaging (transport packaging), which contains an individual antistatic bag and a cardboard box, in the closed transport (automobile, railway, air transportation in heated and pressurized compartments) in storage conditions 5 defined in the IEC 721-2-1 standard (GOST standard 15150-69) or in storage conditions 3 during sea transportation.

The packaged modules should be transported in accordance with the shipping rules, specified for this particular type of transport.

During handling and transportation operations, the packaged modules should not undergo sharp pounding, falls, shocks and exposure to atmospheric precipitation. The goods should be stored in a carrier vehicle in such a manner which will prevent their moving.

Unpacking

Prior to unpacking, after transportation at subzero temperature of ambient air the module(s) should be kept within 6 hours under storage conditions 1 defined in the IEC 721-2-1 standard (GOST standard 15150-69).

It is prohibited to place the packaged module close to the heat source, prior to unpacking.

Retain all original packaging at least until the warranty period is over. You may need it for shipments or for storage of the product.

After unpacking the product, you should inspect it for visible damage that could have occurred during shipping or unpacking. If damage is observed (usually in the form of bent component leads or loose socketed components), contact Fastwel's official distributor from which you have purchased the product for additional instructions.

Storage

Module storage conditions for group 1 are defined in the IEC 721-2-1 standard (GOST standard 15150-69).

MANUFACTURER'S WARRANTY

Warranty Liabilities

The Manufacturer hereby guarantees the product conformity with the requirements of the 4013-025-72782511-09 technical conditions provided that the Consumer complies with the operating, storage, transportation and installation conditions and procedures, specified by the accompanying documents.
The Manufacturer hereby guarantees that the products supplied thereby are free from defects in workmanship and materials, provided operation and maintenance norms were observed during the currently established warranty period. The Manufacturer's obligation under this warranty is to repair or replace free of charge any defective electronic component being a part of a returned product.
Products that broke down through the Manufacturer's fault during the warranty period will be repaired free of charge. Otherwise the Consumer will be invoiced as per the current labor remuneration rates and expendable materials cost

Liability Limitation Right

The Manufacturer shall not be liable for the damage inflicted to the Consumer's property because of the product breakdown in the process of its utilization.

Warranty Period

The warranty period for the products made by Fastwel Group is 24 months since the sale date (unless otherwise provided by the supply contract).
The warranty period for the custom-made products is 36 months since the sale date (unless otherwise provided by the supply contract.

Limitation of warranty liabilities

The above warranty liabilities shall not be applied:
To the products (including software), which were repaired or were amended by the employees, that do not represent the manufacturer. Exceptions are the cases where the customer has made repairs or made amendments to the devices in the strict compliance with instructions, preliminary agreed and approved by the manufacturer in writing;
To the products, broken down due to unacceptable polarity reversal (to the opposite sign) of the power supply, improper operation, transportation, storage, installation, mounting or accident.

Returning a product for repair

1. Apply to Fastwel company or to any of the Fastwel's official representatives for the Product Return Authorization.
2. Attach a failure inspection report with a product to be returned in the form, accepted by the Manufacturer, with a description of the failure circumstances and symptoms.
3. Place the product in the consumer packaging (antistatic bag) and cardboard box, in which the product had been supplied. Failure to package in antistatic material will VOID all warranties of the Customer on a unilateral basis.
4. The customer pays for shipping the product to Fastwel or to an official Fastwel representative or dealer

Notation Conventions

CE Conformity

The CE marking is manufacturer's declaration that this product conforms to the requirements of the applicable EC directives.

Caution: Electric Shock!

This symbol warns about danger of electrical shock (> 60 V) when touching products or parts of them. Failure to observe the indicated precautions and directions may expose your life to danger and may lead to damage to your product. Please also see the below section, dedicated to regulations on operation with high voltage devices.

Warning, ESD Sensitive Device!

This symbol draws your attention to the information related to electro static sensitivity of your product and its components. To keep product safety and operability it is necessary to handle it with care and follow the ESD safety directions. Please also see the below section, dedicated to directions concerning handling the board and unpacking.

Warning!

This sign marks warnings about hot surfaces. The surface of the heatsink and some components can get very hot during operation. Take due care when handling, avoid touching hot surfaces!

Warning!

Information marked by this symbol is essential for human and equipment safety. Read this information attentively, be watchful..

Note

This symbol and title marks important information to be read attentively for your own benefit.

General Safety Precautions

This product was developed for fault-free operation. Its design provides conformance to all related safety requirements. However, the life of this product can be seriously shortened by improper handling and incorrect operation. That is why it is necessary to follow general safety and operational instructions below.

Regulations on safe handling of high voltage

Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.

Caution, Electric Shock!

Before installing this product into a system and before installing other devices on it, always ensure that switched off. This also refers to the installation of mezzanine boards.

Always disconnect external power supply cables during all handling and maintenance operations with t serious danger of electrical shock. This also refers to other lead wires.

Unpacking, Inspection and Handling

Please read the manual carefully before unpacking the module or mounting the device into your syster following:

ESD Sensitive Device!

Electronic modules and their components are sensitive to static electricity. Even a non-perceptible by h discharge can be sufficient to destroy or degrade a component's operation! Therefore, all handling ope this product must be performed with due care, in order to keep product integrity and operability:

n Preferably, unpack or pack this product only at EOS/ESD safe workplaces. Otherwise, it is important to be electrically discharged before touching the product. This can be done by touching a metal part of your system case with your hand or tool. It is particularly important to observe anti-static precautions when setting jumpers or replacing components.

n If the product contains batteries for RTC or memory back-up, ensure that the module is not placed on conductive surfaces, including anti-static mats or sponges. This can cause shortcircuit and result in damage to the battery and other components.

n Store this product in its protective packaging while it is not used for operational purposes.

Unpacking

The product is carefully packed in an antistatic bag and in a carton box to protect it against possible damage and harmful influence during shipping. Unpack the product indoors only at a temperature not less than +15°C and relative humidity not more than 70%. Please note, that if the product was exposed to the temperatures below 0°C for a long time, it is necessary to keep it at normal conditions for at least 24 hours before unpacking. Do not keep the product close to a heat source.

Following ESD precautions, carefully take the product out of the shipping carton box. Proper handling of the product is critical to ensure correct operation and long-term reliability. When unpacking the product, and whenever handling it thereafter, be sure to hold the module preferably

by the front panel, card edges or ejector handles. Avoid touching the components and connectors. Retain all original packaging at least until the warranty period is over. You may need it for shipments or for storage of the product.

Initial Inspection

Although the product is carefully packaged, it is still possible that shipping damages may occur. Careful inspection of the shipping carton can reveal evidence of damage or rough handling. Should you notice that the package is damaged, please notify the shipping service and the manufacturer as soon as possible. Retain the damaged packing material for inspection.

After unpacking the product, you should inspect it for visible damage that could have occurred during shipping or unpacking. If damage is observed (usually in the form of bent component leads or loose socketed components), contact Fastwel's official distributor from which you have purchased the product for additional instructions. Depending on the severity of the damage, the product may even need to be returned to the factory for repair. DO NOT apply power to the product if it has visible damage. Doing so may cause further, possibly irreparable damage, as well as result in a fire or electric shock hazard.

If the product contains socketed components, they should be inspected to make sure they are seated f

Section 1

1. Description and operation of CPB907

1.1. Purpose

CPB907 CPU Module, implemented in the standard COM Express® mini format, provides developers of high-reliable small scale systems with such functions as compatibility with the x86 family, modern set of functional capabilities based on PCI Express / SATA / Gbit Ethernet / USB interfaces, hardware coding / decoding of video, low-energy consumption and ultra-small dimensions, as well as operation in the extended temperature range (-40...+85°C).

The used Intel® Atom™ Queens Bay CPU platform, which contains E6x0T CPU and EG20T controller hub is characterized with high performance, although has a low energy consumption and heat release: E680T (1.6 GHz) TDP = 6 W, E620T (0.6 GHZ) TDP = 4.8 W), as well as announced by manufacturer operation in the extended temperature range (-40…+85ºC). The used solution requires neither a bulky heat-sink nor a forced cooling of the fan) while working in the whole operating temperature range, which is especially important when building the onboard control systems.

The applied COM Express® mini form-factor has ultra-low dimensions (55 84 mm) and uses a standard COM Express® Type10 connector (fully compatible with COM Express® COM.0 Type 10 connector, the CPU& module fully conformal with the "PICMG® COM.0 COM Express® Module Base Specification Revision 2.1").

CPB907 is mainly used as a compute kernel with a wide range of I/O interfaces when building real-time systems, safety and communication onboard systems, video coding and decoding systems, manufacturing control systems, high-speed data acquisition as well as for other critical applications, designed for operation in harsh environments.

The CPB907 CPU Module is installed on the carrier board, which provides access to the main I/O ports. All primary interface signals are routed to the high-density 220-pin connector (3-6318490-6, COM-Express Connector Socket 220-pin Type 10, TYCO).

For more details on COM Express® standard, please visit PICMG® official website at: http://www.picmg.com/.

1.2. General Information

- **CPU:** Intel® Atom™ E6x0T
- Frequency: 0.6 GHz (E620T) / 1.6 GHz (E680T)
- IA32 x86 kernel
- 32 bit memory bus

- Level 1 cache (32 KB)
- Level 2 cache (512 KB)
- Hyper-Threading (2 Threads)
- Intel SpeedStep
- Support of Deep Power Down
- SIMD Extension 2&3 (SSE2, SSE3, SSSE3)

- **Companion chip: Intel EG20T controller hub**

- **RAM:**
- Soldered DDR2-800 SDRAM 1 GB

- **Integrated graphics coprocessor:**
- Frequency: 400 MHz
- 2D/3D acceleration
- Hardware video decoding (H.264, MPEG2, MPEG4, VC1, WMV9)
- Hardware video coding (H.264, MPEG4, H.263) 1
- Independent connection of two displays
- Video memory is allocated from the system memory

- **FLASH BIOS:**
- 1 MB, modifiable within the system and a backup copy

- **Integrated nonvolatile memory:**
- 32 KB FRAM (SPI) for user data (only in CPB907-01/02)
- 8 KB FRAM (I2C) to store configuration
- When there is no battery, the CMOS settings are stored in the FRAM (I2C)

- **FLASH-drive (only in CPB907-01):**
- Connected to SATA interface (SATA1 port)
- 4 GB NAND Flash (SLC)
- Reading / writing speed - 100 / 80 MB/s
- Integrated wear control system and ECC

- **Connector for MicroSD cards:**
- Support of SD cards, SDHC, speed class 6

- **Hardware monotor:**
- Module and CPU temperature monitoring (-55 … +125°C)
- Monitoring of principal supply voltages
- External fan control

- **Digital accelerometer (only in CPB907-01/02):**
- measuring acceleration along 3 axes
- Resolution: 14 / 8 bit
- Programmable measuring range ±2g / ±4g / ±8g/
- Determination of events: free fall, movement, shaking, changing spatial orientation
- Generation of event trapping

- **Digital pressure indicator (only in CPB907-01/02):**
- Pressure measuring range: 50 … 115 KPa
- Conversion range: 1 ms
- Resolution: 0.15 KPa

1 only for CPB907-01, CPB907-02 (is stipulated by E620T CPU limitations)

- standard measurement accuracy ±1 KPa (at the temperature from -20 to +85°C, calibration testing during manufacturing of a microchip, fractional error is not rated).

- **Signals of COM Express® Type 10 connector:**
- 3x ports PCIe x1 (PCIe Spec. Rev 1.0a), 2.5 GB/s;
- 6x ports USB 2.0 (host);
- 1x port USB 2.0 (client);
- 2x ports SATA II (1.5-Gbps Gen. I & 3-Gbps Gen II); [2]
- Port "LAN 0": Gbit Ethernet;
- Port SPI (External Boot);
- Port "LVDS Ch. A": 18/24-bit, 1280x768 @ 60Hz;
- Port DDI: SDVO, 1920x1080 @ 50Hz;
- Port LPC (Spec. Rev. 1.1);
- Port SMBus (Spec. Rev. 2.0);
- Port I2C;
- Port HD Audio;
- Port "Speaker Out";
- Port SDIO (compatible with GPIO ports);
- Port RS-232 (CMOS 3.3V, 256-byte FIFO, up to 4xMbps);
- Port RS-232 (CMOS 3.3V, 64-byte FIFO, up to 1xMbps) or CAN 2.0B Active (CMOS 3.3V, up to 1xMbps);
- Port "RTC battery".

- **Real -Time - Clock** [3]

- **Watchdog timer:**
- CPU integrated – 1 µs …10 minutes
- **OS compatible:**
- Microsoft™ MS-DOS®6.22, FreeDOS
- Linux 2.6
- QNX 6.4x
- Microsoft™ Windows® CE 6.0
- Microsoft™ Windows® XP (Embedded)
- Microsoft™ Windows® 7 (Embedded)
- **console ports: COM1 / COM2**

- **Supply voltage:**
- +4.75…+20.0 V (primary)
- +5 V ±5% (Standby mode S3) [4]
- Short circuit and overvoltage protection.

[2] only SATA0 for CPB907-01 (SATA1 port in version CPB907-01 is occupied by the integrated SATA SSD)
[3] The battery is not included into the delivery checklist of CPB907, for operation of real-time clock it is required to install the battery or other uninterruptable power supply on the carrier-board.
[4] Availability of a voltage source for standby mode 5 V (Standby) is not obligatory for module's operation.

- **Consumed power:**
- 9.0 W for CPB907-01/-02 (operating mode, 12V @ 0.75A);
- 7.5 W for CPB907-03 (operating mode, 12V @ 0.62A);
- 1 W (standby mode, 5V @ 0.2A).

- **Operating temperature range:**
- -40°C … +85°C;

- **Humidity:**
- 5% … 95%, at +25°C without condensation;

- **Shock-/ Vibration resistance:**
- 50g / 5g
- **(MTBF):**
- No less than: 200 000 hours [5]
- **Dimensions:**
- No more than: 55.0 × 84.0 × 15.0 mm;

- **Overall height, with cooling system** (from the bottom surface of module plate to the upper surface heat-distributing plate or heat-sink)**:**
- 13.0 mm (heat-distributing plate is installed, complies with the COM Express v2.1 specification);
- 15.0 mm (finned heatsink is installed);

- **Module weight:**
- No more than 45 g.;

- **Weight of the module with cooling system:**
- No more than 125 g (heat-distributing plate is installed)
- не более 145 г (установлен радиатор с оребрением)

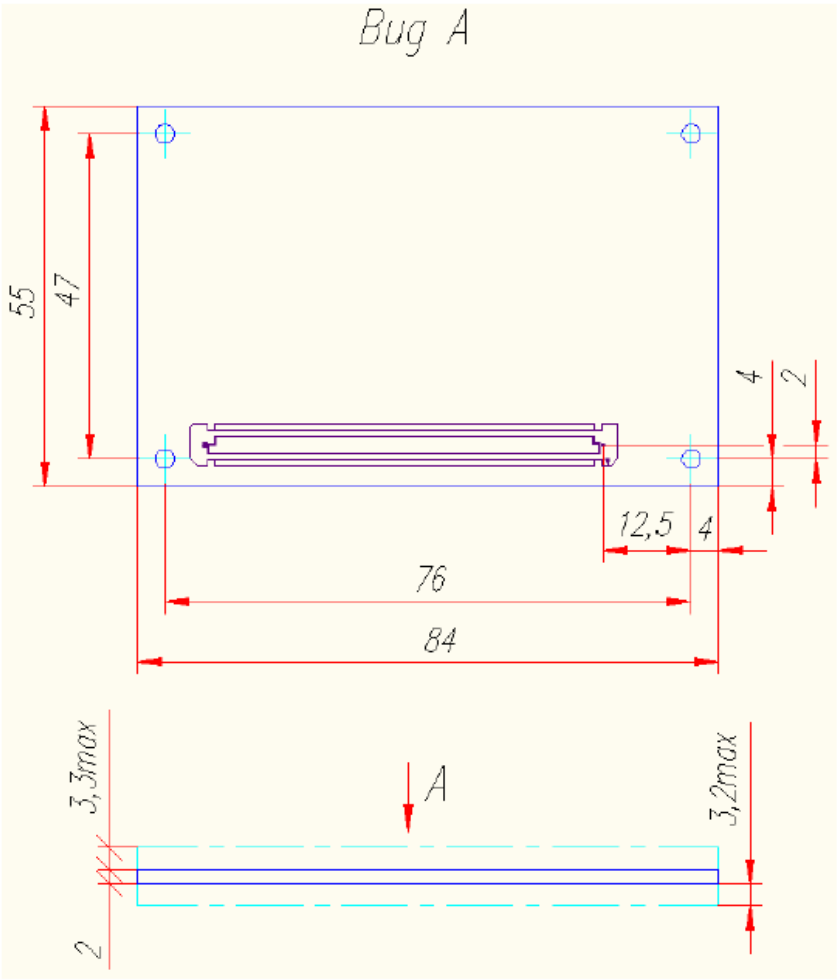
[5] The value is calculated according to: Telcordia Issue 1 model, Method I Case 3, for continuous operation at a surface location, under normal environmental conditions (Moderately Cold climate 4) and at ambient temperatures 30°C.

1.3. Dimensions

This subsection specifies overall and fitting dimensions of CPB907 and carrier-board. Maximum allowed height of components, installed on the upper side of the carrier-board directly under CPB907, amounts to:

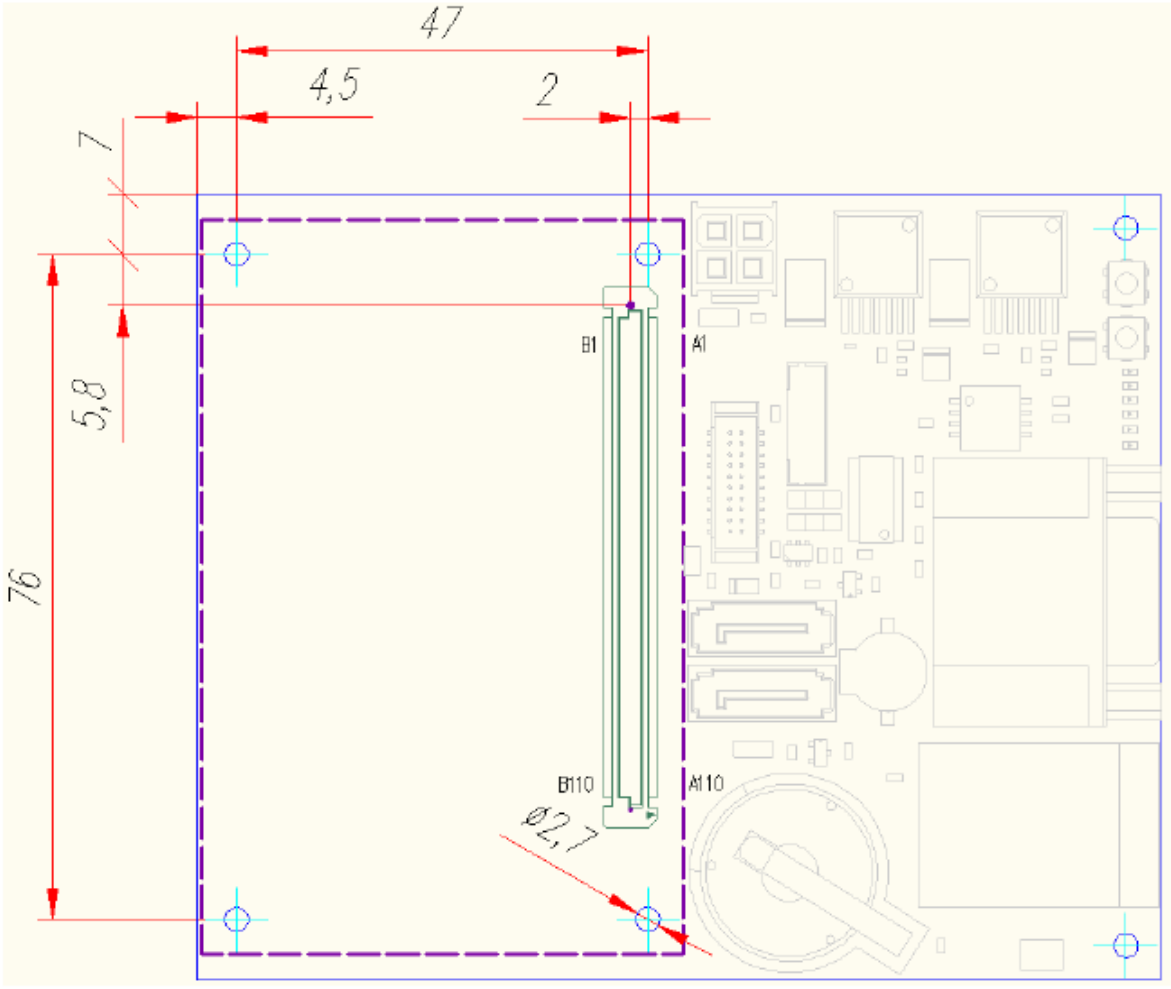
- 5 mm when there is an 8 mm mating COM Express connector (3-6318491-6, TYCO) installed on the carrier-board;
- 2 mm when there is an 8 mm mating COM Express connector (3-1827253-6, TYCO) installed on the carrier-board.

Fig. 1-1: Overall and fitting dimensions of CPB907 (bottom and side view)



This figure shows CPB907 module as viewed from the side of the primary COM-Express Connector Socket 220-pin.

Fig. 1-2: Overall dimensions of the carrier-board's installation spot



This figure with dotted lines shows the location of CPB907 on the carrier-board, as well as overall dimensions of the installation spot.

1.4. Module power supply

Module power supply should correspond to the requirements, specified in the table 1-1. Power is supplied to the module via COM Express connector.
The power supply source should ensure starting current and load current, specified in the table below depending on the module version (starting currents and load currents are specified at rated voltage values). When choosing the power supply, it is required to consider starting current of CPB907 and consumption current of mezzanine modules as well as other devices, connected to the ports of CPB907. Input "+12 V" is equipped with short-circuit (7.5 A) and overvoltage protection (up to 25 V).

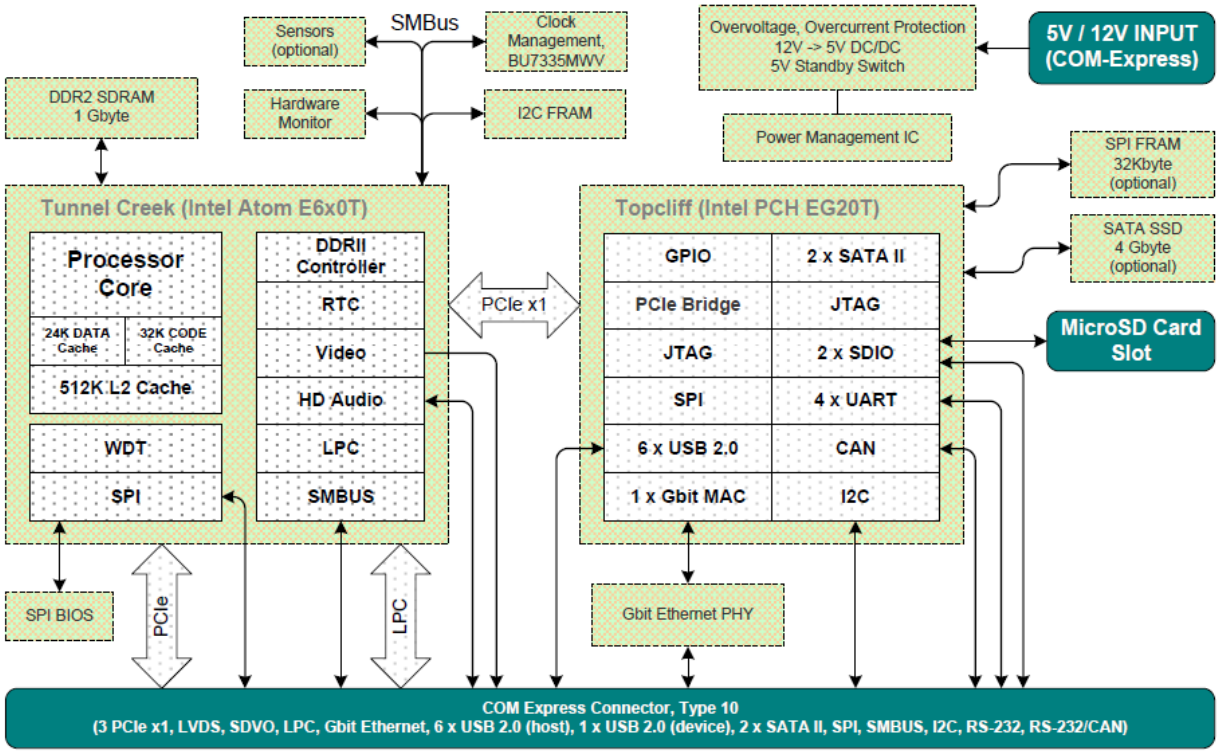
Table 1-1: Requirements for power supply parameters

Version	Power supply voltage, V	Voltage limit values, V	Load current, A	Starting current
CPB907-01 CPB907-02 CPB907-03	+5 (Standby)	от +4.75 до +5.25	0.15 @ 5 V	0.5
	+12	от +4.75 до +20	2.0 A @ 5 V 0.8 A @ 12 V 0.5 A @ 20 V	2.0

* Consumption current information is preliminary.

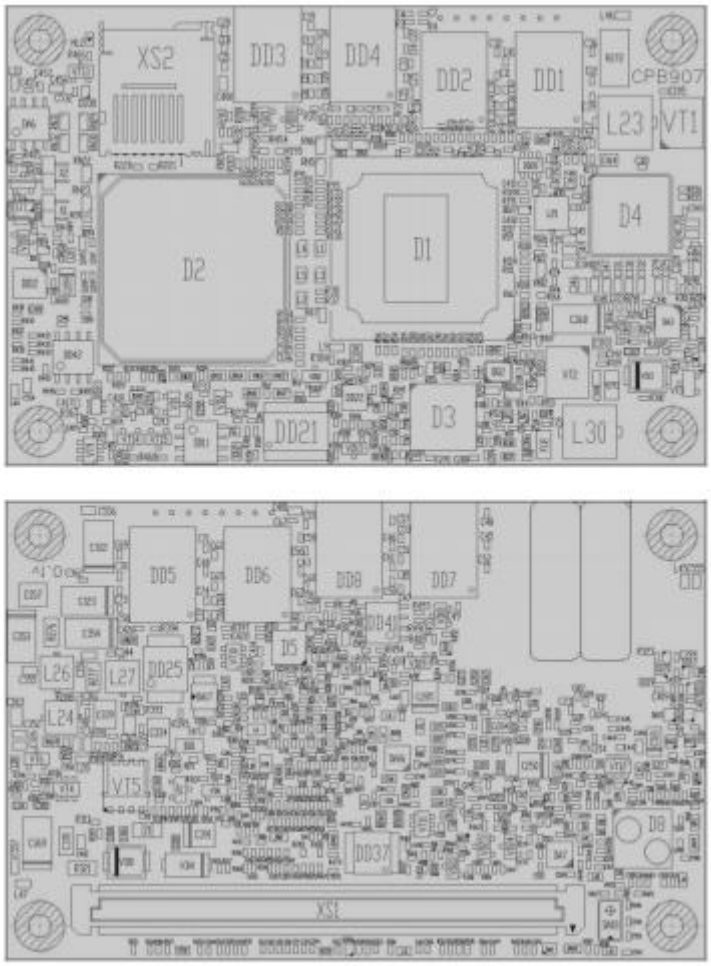
1.5. Block diagram of CPB907

Fig. 1-3: Block diagram of CPB907



1.6. Location of main components of CPB907

Fig. 1-4: Location of main components of CPB907

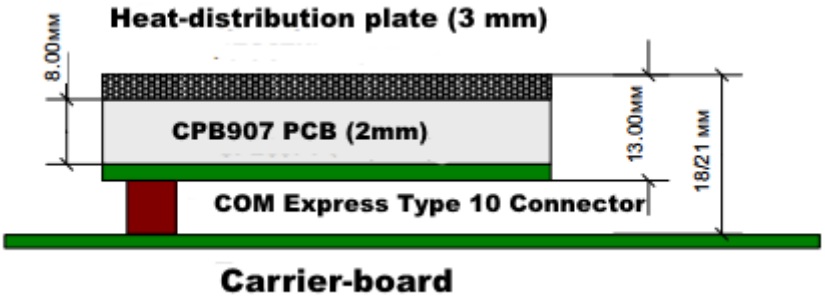


Location of the module's components can differ from the one on the figure.

Purposes of module's connectors are described in the Section "Integral parts of CPB907" and in section Tables of module's connector's contacts.
Purposes of X1…X2 switches are specified in the section Installation of module's switches.

1.7. Installation of CPB907 onto the carrier-board, cooling system

Fig. 1-5: Installation of CPB907 onto the carrier-board



The heat-distribution plate (order number code contains "-R1") is mounted on the top side of the board in accordance with the COM Express specification. The maximum height of components on the top side of the CPB907 board is defined by the COM Express standard and amounts to 5 mm.
The CPB907 module comes with a heat-distribution plate or a heat-sink with fins. The maximum overall height of the module with the installed heat-distribution plate (exclusive of COM Express connector) is 13 mm.
Heat is transferred to the heat-distribution plate is transferred from the following microchips: E6x0T CPU, EG20T controller hub, power management integrated circuits (PMIC), DDR2 memory chips mounted on the top side of the CPB907 board.
Additionally, the heat-distribution plate enables to mount a heat-sink on it.
The maximum height of the heat-sink amounts to 8 mm, thermal resistance of the heat-sink is equal to 5 C/W (without forced cooling /fan). The heat-sink is supplied as an optional accessory (ACS30067). When installing the hat-sink from a kit ACS30067 onto the heat-distribution plate, the total overall height of the module (exclusive of COM Express Connector) will be 21 mm.
It is also possible to include a heat-sink with ribs into the delivery package instead of the heat-distribution plate (order number code contains "-R2"), ensuring the module operation in the entire temperature range without setting an additional heat-sink and heat transfer to the enclosure. When using the
"-R2" ribbed heat-sink, a total overall height of the module (exclusive of COM Express Connector) is 15 mm.

Fig. 1-6: Dimensions of the heat-dissipation plate

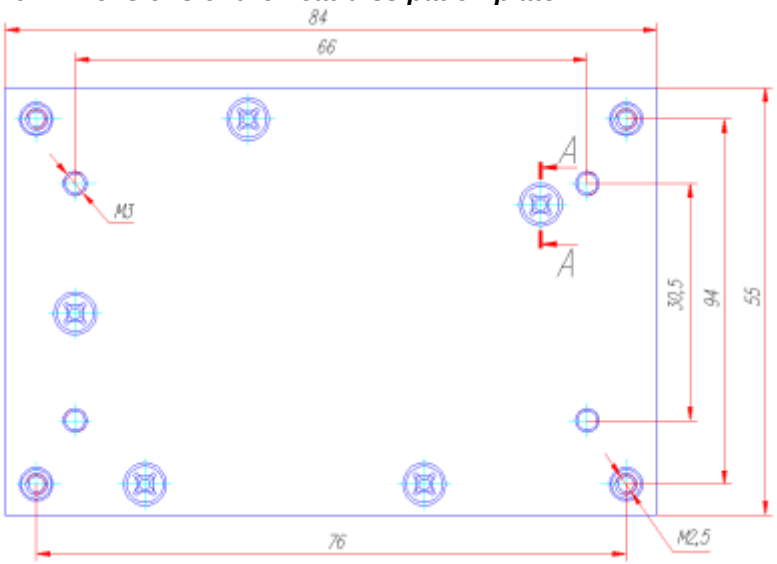
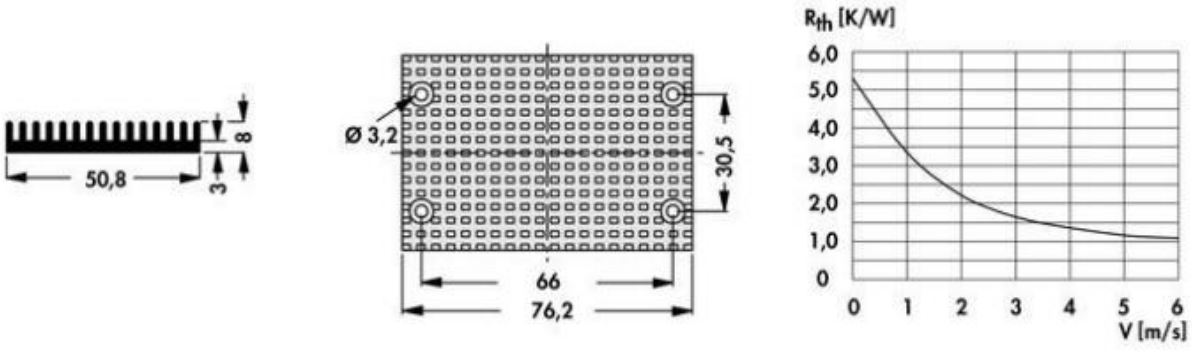


Fig. 1-7: Overall Dimensions of heat-sink (ACS30067) and dependency of its heat-transfer on the generated power and air-flow rate



1.8. Versions

CPB907 CPU module has six major versions.

SPB907-01-E1.6-RAM1024-SSD4G-R1-I - CPB907 CPU Module (COM Express® mini, Type10), Intel E680T 1.6 GHz, 1 GB DDR2 SDRAM, 4GB SSD, slot MicroSD, FRAM 32 KB, accelerometer, pressure sensor, heat-distribution plate.

SPB907-01-E1.6-RAM1024-SSD4G-R2-I - CPB907 CPU Module (COM Express® mini, Type10), Intel E680T 1.6 GHz, 1 GB DDR2 SDRAM, 4GB SSD, slot MicroSD, FRAM 32 KB, accelerometer, pressure sensor, heat-sink with fins.

SPB907-02-E1.6-RAM1024-R1-I - CPB907 CPU Module (COM Express® mini, Type10), Intel E680T 1.6 GHz, 1 GB DDR2 SDRAM, a slot MicroSD, FRAM 32K, accelerometer, pressure sensor, the heat-distribution plate.

SPB907-02-E1.6-RAM1024-R2-I - CPB907 CPU Module (COM Express® mini, Type10), Intel E680T 1.6 GHz, 1 GB DDR2 SDRAM, a slot MicroSD, FRAM 32K, accelerometer, pressure sensor, heat-sink with fins.

SPB907-03-E0.6-RAM1024-R1-I - CPB907 CPU Module (COM Express® mini, Type10), Intel E620T 600 MHz, 1 GB DDR2 SDRAM, a slot MicroSD, heat-distribution plate.

SPB907-03-E0.6-RAM1024-R2-I - CPB907 CPU Module (COM Express® mini, Type10), Intel E620T 600 MHz, 1 GB DDR2 SDRAM, a slot MicroSD, heat-sink with fins.

Differences of versions are summarized in the table below:

Table 1-2: Options of CPB907 Module (differences of the supplied versions)

Order number	CPU	Non-volatile memory	Integrated SSD	SATA ports	Sensors	Cooling system in kit
CPB907-01-E1.6-RAM1024-SSD4G-R1-I	E680T, 1.6 GHz	FRAM 32 KB	4GB	1 x port (COM Express)	Acceleration and temperature sensors	Heat-distribution plate
CPB907-01-E1.6-RAM1024-SSD4G-R2-I						Heat-sink with fins
CPB907-02-E1.6-RAM1024-R1-I			-	2 x ports (COM Express)		Heat-distribution plate
CPB907-02-E1.6-RAM1024-R2-I						Heat-sink with fins
CPB907-03-E0.6-RAM1024-R1-I	E620T, 0.6 GHz	-			Temperature sensors	Heat-distribution plate
CPB907-03-E0.6-RAM1024-R2-I						Heat-sink with fins

Options available:

PRE-INSTALLED OPERATING SYSTEM*	
\WCE6	Windows CE 6.0
\LNX	Linux 2.6
\WXPE	Windows XP Embedded

COATING	
\COATED	*Conformal coating*

* Information on the availability of pre-installed QNX operating system is provided upon individual request.

** If the module is ordered without any kits, it is required to specify "\OEM" option at the time of order.

1.9. Delivery checklist

Standard delivery checklist of CPB907 CPU Module includes:

1. CPB907 Module;
2. Heat-distribution plate / Heat-sink with fins;
3. Assembly kit for installation of COM Express mini modules onto the carrier-board (5 and 8 mm);
4. Package.

1.10. Additional accessories

Table 1-3: Additional accessories for CPB907 CPU Module

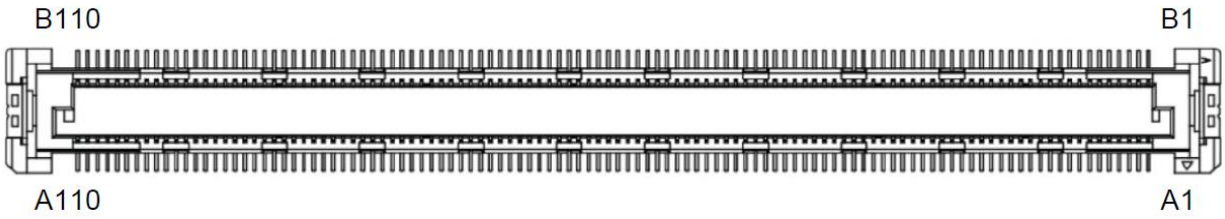
KIB1283-02	Developer's kit for COM Express mini modules
ACS30067	Heat-sink for COM Express mini modules (installed onto the heat-distribution plate)

1.11. Component parts of CPB907

1.11.1. Main high-density COM Express connector (XS1)

All primary interfaces are routed to 220-pin high-density connector (3-6318490-6, COM Express Connector Socket 220-pin Type I, TYCO). Below is the view from the back of the CPB907 board, overlooking the COM Express connector.

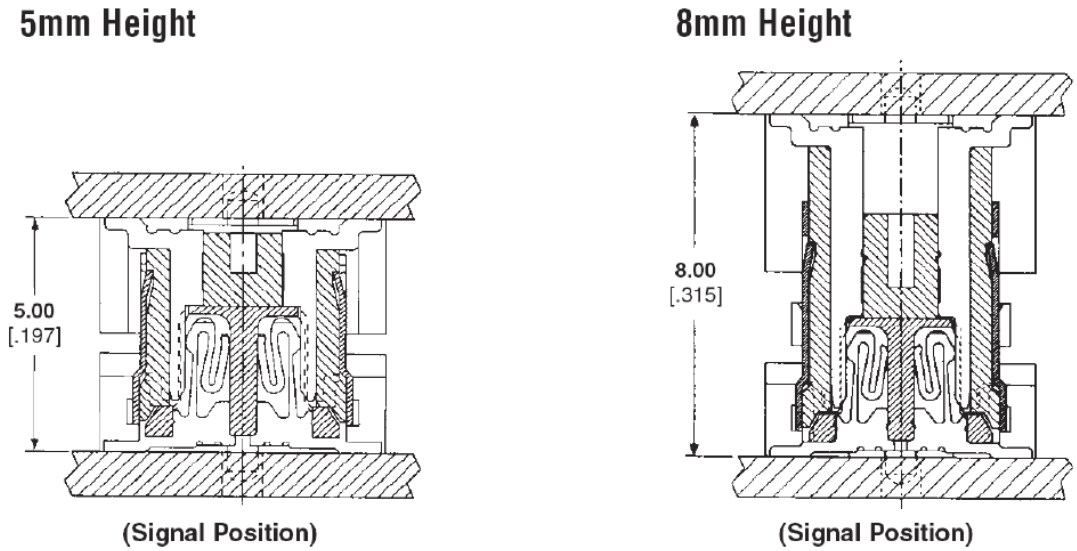
Fig. 1-8: Main 220-pin high-density connector of CPB907 module (viewed from the bottom of CPB907).



As a counterpart of the COM Express connector, it is recommended to use on the carrier-board:

- 3-1827253-6 (TYCO) – distance between the CPB907 board and the carrier-board: 5 mm
- 3-6318491-6 (TYCO) – distance between the CPB907 board and the carrier-board: 8 mm.

Fig. 1-9: Connection of the COM-Express CPB907 and counterpart of the carrier-board



1.11.2. E620T / E680T CPU

CPB907 is built on the basis of x86-compatible 32-bit Intel® Atom™ E620T / E680T CPU (depending on CPB907 version), manufactured on the basis of 45 Nm technology, with low power consumption and industrial operating temperature range (-40 … +85ºC). Operating clock frequency – 600 MHz (E620T) /1.6 GHz (E680T). For more information please visit manufacturer's website at: http://ark.intel.com/ru/products/series/52490.

It represents a highly-integrated solution, combining Intel® Atom™ core, 32-bit DDR2 SDRAM memory controller (up to 2 GB, 400 MHz), graphics subsystem with 2D/3D acceleration (video processor frequency: 400 MHz), extension buses 4 PCIe x1 (1.0a) and LPC (1.1), High Definition Audio subsystem, SMBus, SPI, up to 14 GPIO lines, Real Time Clock. The CPU has implemented a hardware support of video coding (MPEG-4 / H.263 / H.264 – only in E680T), as well as hardware acceleration of video decoding (H.264 / MPEG2 / MPEG4 / VC1 / WMV9 – in E620T and E680T).

1.11.3. EG20T Controller Hub

The module uses Intel® EG20T (Topcliff) controller hub, manufactured in accordance with 90 Nm technology, with low power consumption and industrial temperature range (-40 … +85ºC). For exchanging data with CPU PCIe x1 bus will be used. EG20T represents a highly-integrated controller of such interfaces as: 6 x USB 2.0 (host), USB 2.0 (device), Gbit Ethernet (MAC), 2 x SATA II, 2 x SDIO, SPI, I2C, 4 x UART, CAN.

1.11.4. Random Access Memory (RAM)

As system memory, the CPB907 module uses 1GB DDR2 SDRAM operating at a frequency of 400 MHz.

Installation of memory extension module is not provided.

1.11.5. FLASH BIOS Read-Only Memory

In order to store the Basic I/O system (hereinafter referred to as the BIOS), the module uses 2MB SPI-FLASH (SST25VF016B).

Loading from and external SPI-FLASH microchip installed onto the carrier board, is supported too.

1.11.6. Non-Volatile Memory

For storing user data in the module, FRAM 32 KB (Ramtron, FM25L256) non-volatile memory is provided, and is will be used as a replacement for a standard non-volatile random access memory. For exchanging data with SPI FRAM 32 KB, SPI interface of EG20T chipset will be used. Manufacturer guarantees 100 trillion read/write cycles, which, within such application mode, will be equivalent to ~ 340 years of application (in case of continuous cyclic write-read procedure).

For storing this configuration, a separate 8 KB FRAM non-volatile memory will be used, which is connected to the CPU SMBus interface. If there is no battery, CMOS settings will be stored in FRAM. This memory could be additionally used for storing calibration factors of acceleration sensor.

A separate 512 Kb 25LC512-I/SN microchip of EEPROM memory will be used for storing MAC-address of Gbit Ethernet controller integrated into EG20T chipset.

1.11.7 RTC, CMOS

Real-time clock is integrated into CPU. In case of the switched off power supply, clock operability is ensured via "RTC battery" port of COM-Express connector, from the carrier-board. Battery current consumption amounts to 12 μA (standard value), which corresponds to 2 years of use from a standard CR2032 lithium-battery of 220 mAh, provided that the module has been in off state for 24 hours (battery should be installed into the carrier-board). However, an actual battery service life relies heavily on ambient temperature, as well as on the fact, how long time system has been off.

Note:
It is recommended to change the battery each 2 years of operation,
not awaiting its end of life.

Note:
When changing battery, observe the polarity (“+” should be on top).
The used battery should be disposed in accordance with the established regulations.

BIOS settings are stored in a separate non-volatile memory FRAM (8 KB).

1.11.8. Slot for MicroSD cards

The module enables the use of MicroSD Card as drive (SDSC, SDHC, Spec. v1.1, v2.0), for this purpose, the top side of the board has a relevant MicroSD (XS2) connector.
"Push-Push" socket (DM3B-DSF-PEJ, Hirose) is used. This type of connector allows for a horizontal card removal. The connector located in such a way that availability of a heat-distribution plate or heat-sink would not prevent removal of the MicroSD card.

1.11.9. Integrated SATA SSD

As an option (only in the delivered configuration CPB907-01), the module is equipped with 4GB SATA SSD (port SATA1 of EG20T controller hub). Controller and 2 microchips SLC NAND Flash are integrated in a single chip.
Read / write speed is 100 / 80 MB/s, there is an integrated wear control system and hardware error correction mechanism ECC (8/15 bit to 512 byte, 16/30 bit to 1 KB). MTBF of the drive amounts to 2 000 000 hours.

1.11.10. PCI Express port (XS1)

3x ports PCIe x1 are routed to the COM Express connector. Specification PCIe Spec. Rev 1.0a is supported, data exchange speed – up to 2.5 GB/s.

1.11.11. SATA port (XS1)

2x SATA ports (in the delivered configuration CPB907-01 there is only 1x SATA port (SATA0) available, since SATA0 port in CPB907-01 is used for the connection of integrated 4 GB SSD), are routed to the COM Express connector. Support of SATA I, SATA II specifications. SATA0/SATA1 ports of EG20T controller hub are used.

1.11.12. USB 2.0 port (XS1)

The module has 6 x USB Host ports, as well as 1x USB Device port with support of USB 1.1 and USB 2.0 specifications. The USB ports are routed to the COM Express connector.

1.11.13. Gbit Ethernet port (XS1)

The module has 1x Gbit Ethernet port. Gigabit Ethernet MAC controller integrated into the controller hub is used. 88E1510-A0-NNB2I000 (Marvell) is used as PHY. Port is routed to the COM Express connector. Support of the following operation modes: 10/100/1000 Mb.

1.11.14. COM1 / COM2 (XS1) serial ports

The CPU module has two asynchronous serial ports: COM1 and COM2. COM1 – 2-wire interface UART (CMOS, 3.3V), speed up to 4Mb/s, FIFO buffer 256 byte (EG20T, UART0). COM2 – 2-wire interface UART (CMOS, 3.3V), speed up to 1Mb/s, FIFO buffer 64 byte (EG20T, UART1) or CAN 2.0B (CMOS, 3.3V), speed up to 1Mb/s (EG20T, CAN-port). Configuration of the port (UART or CAN) is selected by software, using BIOS Setup settings, by default - UART.
The both ports are routed to the COM Express connector and can be used for console input/output and loading files (COM1 port will be used as a console port, by default).
Overvoltage protection up to 14 V (which is associated with COM-Express Type 1 and Type 10 compatibility requirements) is implemented.
The UART ports are fully software-compatible with the UART 16550 version.
CAN port is compatible with "BOSCH CAN Protocol Version 2.0B Active" (standard and extended format) in accordance with ISO 11519, ISO 11898, and SAEJ2411.
In order to enable the ports to operate within networks RS-232, RS-422/485 or CAN it is required to equip the carrier-board with relevant transmitter-/receiver units.
Data exchange speed over serial ports can be set in the BIOS Setup settings. The data exchange speed is determined by the value of CPU frequency divider register. The divider's value will be calculated according to the following formula:

DIV = F / BR, BR=F / (DIV×16)
where

- F – is an internal generator's frequency [MHz];

F = (12.288, 25, 48) ×PLL2VCO×BAUDDIV (PLL2VCO = 1…6, BAUDDIV = 1…16) maximum value F = 192 MHz

- DIV – divider's value (minimum value DIV = 1);
- BR – exchange rate required [bit/s].

Attention!
The receiver tolerates deviations of data exchange rate by 3,0% downward and by 2,5% - upward.

The below table has values frequency divider for a number of data exchange rates:

Table 1-4: Values of frequency dividers for serial ports

Exchange rate, bit/s.	F=175 MHz	(CLK=25 MHz MPLL2VCO=7, BAUDDIV=1)	F=25 MHz	(CLK=25 MHz PLL2VCO=1, BAUDDIV=1)	F=48 MHz	(CLK=25 MHz PLL2VCO=1, BAUDDIV=1)
	Divider	Error, %	Divider	Error, %	Divider	Error, %
300	36458	- 0.001	5208	- 0.006	10000	0.000
600	18229	- 0.001	2604	- 0.006	5000	0.000
1200	9115	+ 0.005	1302	- 0.006	2500	0.000
2400	4557	- 0.006	651	- 0.006	1250	0.000
4800	2279	+ 0.016	326	+ 0.147	625	0.000
7200	1519	- 0.006	217	- 0.006	417	+ 0.080
9600	1139	- 0.028	163	+ 0.147	313	+ 0.160
14400	760	+ 0.059	109	+ 0.452	208	- 0.160
19200	570	+ 0.059	81	- 0.469	156	- 0.160
28800	380	+ 0.059	54	- 0.469	104	- 0.160
38400	285	+ 0.059	41	+ 0.756	78	- 0.160
57600	190	+ 0.059	27	- 0.469	52	- 0.160
115200	95	+ 0.059	–	–	26	- 0.160
230400	47	- 1.004	–	–	13	- 0.160
256000	43	+ 0.640	6	- 1.725	12	+ 2.343
312500	35	+ 0,000	5	0.000	–	–
460800	24	+ 1,100	–	–	–	–
921600	12	+ 1,100	–	–	–	–
1843200	6	+ 1,100	–	–	–	–
1000000	11	+ 0,568	–	–	3	0.000
1500000	–	–	–	–	2	0.000
3000000	–	–	–	–	1	0.000

1.11.15. LVDS and SDVO ports (XS1)

For connection of LCD(TFT)-panels, LVDS interface is used. This interface is routed to the COM Express connector. Color depth may amount to 24 bits (18-bit mode is also supported). Maximum resolution: 1280 x 768 @ 60Hz. LVDS interface may be routed directly to the LVDS connector on carrier-board.

SDVO interface is also routed to the COM Express connector. Maximum resolution: 1920 x 1080 @ 50Hz. For connection of the video units, the carrier-board should be equipped with a relevant converter: SDVO – CRT (e.g. CH7317B Chrontel), SDVO – DVI, SDVO – HDMI, SDVO – LVDS (e.g. CH7308B Chrontel).
Independent operation of two displays is supported.
For operation of LVDS-panel or other video output devices in Linux, WindowsXP, Windows7 operating systems, it is required to use Intel IEMGD suite, which latest version can be downloaded from the official website at: http://www.intel.ru.

1.11.16. HDA port (XS1)

For connection of audio devices, High Definition Audio interface (controller is integrated into the EG20T controller hub) is routed to the COM Express connector.
Operation of the audio port requires the carrier board to have a relevant audio codec (e.g. CS4207 Cirrus Logic) installed.

1.11.17. SDIO / GPIO port (XS1)

GPIO port of the controller hub (EG20T) is used. The port is intended for input/output of 8 logic signals. Interrupt generation becomes possible over each of the GPIO lines.
The port is software-compatible with SDIO port, on COM Express connector (CMOS level, 5V Tolerant).
Port configuration is software-selectable, in BIOS Setup settings (GPIO port, by default).

1.11.18. Acceleration, pressure and temperature sensors, hardware monitor

A capacitive micromachined accelerometer MMA8451Q (Freescale) is used as acceleration sensor[6].This device, having 8/14 bit resolution, enables to measure acceleration along three axes, вибраций в диапазонах 2/4/8 g, determine slope angle, free fall, detect pulse and jolts. Relative measurement errors are not rated.

The module is also equipped with a Miniature I2C Digital Barometer [7] MPL115A2 (Freescale), which provides accurate pressure measurements from 50 to 115 kPa (standard measuring precision is 1 kPa, with the operating temperature range that spans from -20 to +85°C, resolution of 0.15 KPa). Calibration of the device is carried out by the manufacturer during production process. Relative measurement errors are not rated.
The acceleration and pressure sensors are connected to SMBus of the CPU and enable generating system interrupts for events. The measurement errors are not rated, the standard measurement errors are defined by characteristics, stated by device manufacturers.
The used LM87 and LM96163 hardware monitors enable to control module's main voltages, module's and CPU temperature, as well as to control an external fan.

6 only in CPB907-01, CPB907-02
7 only in CPB907-01, CPB907-02

1.11.19. Watchdog timer

The module uses 1 hardware watchdog timer, integrated into the processor chip, with the modifiable actuation range from 1 μs to 10 minutes.
A logic signal of watchdog timer actuation (CMOS, 3.3B - при срабатывании сторожевого таймера состояние линии переходит в логическую единицу) is routed to the COM Express connector.

1.11.20. Reset and power supply monitoring

Module reset signal is generated from the following sources:

From supervisor at the time of power up;

From the external reset signal from the COM Express connector;

From the watchdog timer.

CPU switch from the standby mode (from S3 state to S0 state) can be carried out from the following sources, from COM Express connector:

Gbit Ethernet 0 port (Magic Packet);

COM1 port;

GPIO port;

USB port;

WAKE# signal.

1.11.21. LPC port (XS1)

LPC port includes all signals of LPC extension bus, except for DRQ signal and is routed to the COM Express connector (direct access mode is not supported by LPC bus controller).
Support of LPC Rev 1.1. specification.

1.11.22. SMBus and I2C ports (XS1)

SMBus CPU port is routed to the relevant port of COM Express connector. Additionally, lines of I2C interface of EG20T controller hub are routed to the COM Express connector.

1.11.23. PC-buzzer port (XS1)

PC-buzzer port is routed to the COM Express connector.

1.11.24. LEDs

Table 1-5: Purpose of CPB907 LEDs

LED	Function
HL1	Diagnostic input power supply LED (green)
HL2	LED of module's MicroSD card activity (green)
HL3	LED of integrated SATA SSD activity (green)

During module's normal operation, after power-up, the HL1 LED is lighted with green. HL1 is off when there is a short circuit or there is no input power supply voltage of "12 V".
The HL2-HL3 LEDs are flashing when addressing to the relevant devices.

SECTION 2

TECHNICAL CHARACTERISTICS

2. Technical specification

Table 2-1: Requirements for electric power supply of CPB907

Electric supply requirements	
Power supply voltage “+ 12V” (principal voltage)	+12 V (+4.75 … +20 V)
Power supply voltage "+5 V" STANDBY (standby mode)	+5 V (+4.75 … +5.25 V)[8]
Consumption current over power supply voltage, no more than:	
CPB907-01, CPB907-02	1800 mA @ +5V (9.0 W) 750 mA @ +12V (9.0 W) 450 mA @ +20V (9.0 W) 200 mA @ +5V STANDBY (1 W)
CPB907-03	1500 mA @ +5V (7.5 W) 625 mA @ +12V (7.5 W) 375 mA @ +20 B (7.5 W) 200 mA @ +5 B STANDBY (1 W)
Maximum available current consumed over external circuits (standard value at +25C, limited by the installed resettable fuse):	
SPI_POWER (XS1)	100 mA

Table 2-2: Characteristics of GPIO

Digital I/O	
Output voltage, Logical 1	max. 3.3 V
Input voltage, Logical 0	max. 0.8 V
Input voltage, logical 1	min. 2.0 V, max. 5.5 V
Output voltage, Logical 0 (at the current of 8 mA)	max. 0.4 V
Output voltage, Logical 1 (at the current of 8 mA)	min. 2.4 V

Table 2-3: Characteristics of serial ports

Serial ports	
Maximum exchange rate via COM1 serial port (UART)	4 Mb/s
Maximum exchange rate via COM2 serial port (UART)	1 Mb/s
Maximum exchange rate via COM2 serial port (CAN)	1 Mb/s

[8] Additional power supply voltage +5 B STANDBY is not necessary for module’s operation

Table 2-4: Characteristics of SATA port

SATA port	
Number of external SATA devices	Up to two devices SATA0, SATA1 ports
Supported operation modes of SATA devices	SATA Gen.1 (1.5 Gb/s), SATA Gen.2 (3.0 Gb/s),
Volume of the integrated SSD (SATA1 port)[9]	4 GB (NAND Flash, SLC) with the integrated wear control system and hardware error correction mechanism ECC (8/15 bit to 512 byte, 16/30 bit to 1 KB). MTBF of the drive amounts to 2 000 000 hours.

Table 2-5: Characteristics of USB, Ethernet ports

USB, Ethernet ports	
Type of USB ports	USB Host, 6x ports USB Device, 1x port
Types of supported USB-devices	1.1, 2.0
Exchange rate over Ethernet channel	10/100/1000 Mb/s
LED indication of Ethernet-channel activity	LEDs on the carrier-board: Activity (ACTIVE) and communications link state (LINK).

Table 2-6: Mechanical characteristics

Mechanical characteristics	
Vibration resistance	5 g (acceleration amplitude)
Single shock resistance	100 g (peak acceleration)
Multiple shocks resistance	50 g (peak acceleration)
Overall dimensions of module, no more than	55 84 15 mm
Overall height of the module with cooling system, exclusive of COM Express connector	13 mm (corresponding to the COM Express specification)
Module weight, no more than	45 g (without MicroSD card and heat distribution plate)
Module weight with cooling system, no more than	125 g (heat distribution plate is installed) 145 g (finned heat-sink is installed)
MTBF [10]	No less than 200 000 hours

[9] Only for the version CPB907-01.

[10] MTBF values are calculated according to the Telcordia Issue 1 model, Method I Case 3, for continuous operation, located on the ground, at normal environmental conditions (Moderately Cold Climate 4, in accordance with the GOST standard 15150-69) and at ambient temperature 30°C.

Table 2-7: Environmental conditions

Environmental conditions	
Operating temperature range	-40..+85C
Module storage conditions	1 according to the GOST 15150-69 standard
Relative humidity	Up to 80 %, without moisture condensation

2.2. Allocation of hardware interrupts

Table 2-8: Addresses of hardware interrupts

#	Source by default	Alternative sources
NMI	-	Watchdog Timer (WDT)
IRQ0	Reserved (System Time Clock)	-
IRQ1	PS/2 Keyboard	-
IRQ2	Reserved (coding)	-
IRQ3	COM2	-
IRQ4	COM1	-
IRQ5	External devices	-
IRQ6	USB	
IRQ7	External devices	-
IRQ8	RTC	-
IRQ9	External devices	-
IRQ10	External devices	-
IRQ11	External devices	-
IRQ12	PS/2 Mouse	-
IRQ13	Reserved (Coprocessor support)	-
IRQ14	-	-
IRQ15	-	-

2.3. Module’s DMA channels

Table 2-9: Module’s DMA channels

#	
DRQ0	-
DRQ1	External devices
DRQ2	External devices
DRQ3	External devices
DRQ5	External devices
DRQ6	External devices
DRQ7	External devices

2.4. Address I/O space

Table 2-10: Allocation of address I/O space

Address	Function	Notes
0000h – 000Fh	Slave DMA	
0020h – 0021h	Master Interrupt Controller	
0022h – 0023h	Indirect Access	
0040h – 0043h	Timer / Counter	
0048h – 004Bh	PWM Control	
0060h 0064h	Keyboard / Mouse Control	
0061h	NMI Status / Control	
0065h 0067h	WDT Reload	
0068h – 006Dh	WDT Control	
0070h – 0071h	CMOS Memory / RTC	
0072h – 0075h	MTBF	
0081h – 008BFh	DMA Page	
0092h	System Control	
00A0h – 00A1h	Slave Interrupt Controller	
00C0h – 00DFh	Master DMA	
0278h – 027Fh		
0280h – 02BFh		
02E8h – 02EFh		
02F8h – 02FFh	COM2	
03E8h – 03EFh		
03F8h – 03FFh	COM1	
0481h – 0483h 0487h 0489h – 048Bh	DMA High Page	
0490h – 0499h	Interrupt Edge / Level Control	
04D0h – 04D1h	Instruction Counter	
0CF8h – 0CFFh	PCI Configuration	

2.5. Address memory space

Table 2-11: Memory device address

Address	Device	Notes
00000 – 9FFFFh	DOS	DOS Area 640 Kbyte
A0000 – BFFFFh		Область видеопамяти 128 Kbyte
C0000 – CFFFFh		
D0000 – DFFFFh		
E0000 – EFFFFh	System BIOS	Extended System BIOS area 64 KB (16 KB x 4)
F0000 – FFFFFh	System BIOS	System BIOS area 64 KB

Address	Device	Notes
10 0000 – MEMORY TOP *	DRAM	DDR2 SDRAM
MEMORY TOP * – FFE0 0000	PCI	PCI
FFE0 0000 – FFFF FFFFh	High BIOS	High BIOS Area 2 Mbytes (mapped to PCI)

** Set volume DDR2 SDRAM 1024 MB.*

2.6. Use of GPIO ports

Microchip of E6x0T CPU contains 2 I/O ports – GPIO (General Purpose Input / Output), available for the user via microchip's internal registers. The first "GPIO" port represents 5 I/O lines, the second one "GPIO_SUS"– 9x lines each of them can be adjusted as input or output by programming the registers of a relevant port. Lines of "GPIO_SUS" port opposed to the "GPIO" port lines retain their states, if they were adjusted to the output when switching to the standby mode (S3).
In addition, lines of GPIO port of GPIOP[11:0] have been activated. Lines of GPIOP[7:0] are routed to the COM Express connector (multiplexed with SDIO lines).
Purpose of GPIO ports used is given in the table below.

Table 2-12: Purpose of GPIO ports of E6x0T processor

Line of I/O port	Direction of I/O line	Description
GPIO_4	Input / Output	Watchdog timer actuation flag Front – actuation has been carried out
GPIO_3	Input	Configuration of COM2 port (SER1_TX/SER1_RX lines): 1 – CAN interface 2 – UART interface (by default)
GPIO_2	Input	Not used

Line of I/O port	Direction of I/O line	Description
GPIO_1	Input	USB HOST PRESENT (logics for determining USB HOST availability at the time of CPB907 module connection as USB Device, USB OTG mode). 1 – CPB907 USB HOST is connected, 0 – CPB907 USB HOST is not connected.
GPIO_0	Input	Not used
GPIO_SUS_8	Input	Not used
GPIO_SUS_7	Input/Output	Reset of Ethernet PHY controller: 1 – Normal module operation, 0 – Reset. The line is set as input by default.
GPIO_SUS_6	Input/Output	Not used
GPIO_SUS_5	Input	Not used
GPIO_SUS_4	Input / Output	LVDS_I2C_DATA Control of LVDS panel, I2C_DATA signal
GPIO_SUS_3	Output	LVDS_I2C_CLK Control of LVDS panel, I2C_CLK signal.
GPIO_SUS_2	Output	LVDS_BKLT_CTRL Signal of LVDS panel illumination control.
GPIO_SUS_1	Output	LVDS_BKLT_EN Switching on the power of the illumination of LVDS panel.
GPIO_SUS_0	Output	LVDS_VDDEN Switching on the power of the LVDS panel.

Table 2-13: Purpose of GPIO ports of EG20T chipset

Line of I/O port	Direction of I/O line	Description
GPIO_11	Input	Reserved
GPIO_10	Input	Reserved
GPIO_9	Input	CB_BATLOW# 1 – normal module operation, 0 – Low battery charge level.
GPIO_8	Input / Output	Configuration of GPIO port CB_GPIO_SEL# 1 – SDIO interface, 0 – GPIO interface (by default).
GPIOP_7… GPIOP_0	Input / Output	Lines are routed to GPIO port of COM Express connector

2.7 Tables of module connectors contacts [11]

2.7.1 Table of contacts of COM Express Type 10 (XS1)

Table 2-14: Purpose of contacts of COM Express connector (XS1)

XS1: COM Express Connector Socket 220-pin Type I (3-6318490-6, TYCO)					
Contact #	**Purpose**	**Configuration**	**Contact #**	**Purpose**	**Configuration**
B1	**GND (FIXED)**		A1	**GND (FIXED)**	
B2	GBE0_ACT#	Output	A2	GBE0_MDI3-	Input / Output
B3	LPC_FRAME#	Output	A3	GBE0_MDI3+	Input / Output
B4	LPC_AD0	Input / Output	A4	–	–
B5	LPC_AD1	Input / Output	A5	–	–
B6	LPC_AD2	Input / Output	A6	GBE0_MDI2-	Input / Output
B7	LPC_AD3	Input / Output	A7	GBE0_MDI2+	Input / Output
B8	–	–	A8	GBE0_LINK#	Output
B9	–	–	A9	GBE0_MDI1-	Input / Output
B10	LPC_CLK	Output	A10	GBE0_MDI1+	Input / Output
B11	**GND (FIXED)**		A11	**GND (FIXED)**	
B12	PWRBTN#	Input	A12	GBE0_MDI0-	Input / Output
B13	SMB_CK	Output	A13	GBE0_MDI0+	Input / Output
B14	SMB_DAT	Input / Output	A14	GBE0_CTREF	Output
B15	SMB_ALERT#	Input	A15	SUS_S3#	Output
B16	*SATA1_TX+	Output	A16	SATA0_TX+	Output
B17	*SATA1_TX-	Output	A17	SATA0_TX-	Output
B18	SUS_STAT#	Output	A18	SUS_S4#	Output
B19	*SATA1_RX+	Input	A19	SATA0_RX+	Input
B20	*SATA1_RX-	Input	A20	SATA0_RX-	Input
B21	**GND (FIXED)**		A21	**GND (FIXED)**	
B22	–	–	A22	–	–
B23	–	–	A23	–	–
B24	PWR_OK	Input	A24	SUS_S5#	Output
B25	–	–	A25	–	–
B26	–	–	A26	–	–
B27	WDT	Output	A27	BATLOW#	Output
B28	–	–	A28	SATA_ACT#	Output
B29	AC/HDA_SDIN1	Input	A29	AC/HDA_SYNC	Output
B30	AC/HDA_SDIN0	Input	A30	AC/HDA_RST#	Output
B31	**GND (FIXED)**		A31	**GND (FIXED)**	

[11] Hereinafter referred to as: symbol # in the signal name – active logic “0” level.

XS1: COM Express Connector Socket 220-pin Type I (3-6318490-6, TYCO)

Contact #	Purpose	Configuration	Contact #	Purpose	Configuration
B32	SPKR	Output	A32	AC/HDA_BITCLK	Output
B33	I2C_CK	Output	A33	AC/HDA_SDOUT	Output
B34	I2C_DAT	Input / Output	A34	BIOS_DIS0#	Input
B35	THRM#	Input	A35	THRMTRIP	
B36	USB7-	Input / Output	A36	–	–
B37	USB7+	Input / Output	A37	–	–
B38	USB_4_5_OC#	Input	A38	–	–
B39	USBH5-	Input / Output	A39	USBH4-	Input / Output
B40	USBH5+	Input / Output	A40	USBH4+	Input / Output
B41	**GND (FIXED)**		A41	**GND (FIXED)**	
B42	USBH3-	Input / Output	A42	USBH2-	Input / Output
B43	USBH3+	Input / Output	A43	USBH2+	Input / Output
B44	USB_0_1_OC#	Input	A44	USB_2_3_OC#	Input
B45	USBH1-	Input / Output	A45	USBH0-	Input / Output
B46	USBH1+	Input / Output	A46	USBH0+	Input / Output
B47	EXCD1_PERST#	Output	A47	VCC_RTC	Input (power)
B48	EXCD1_CPPE#	Input	A48	EXCD0_PERST#	Output
B49	SYS_RESET	Input	A49	EXCD0_CPPE#	Input
B50	RESET#	Output	A50	LPC_SERIRQ	Input
B51	**GND (FIXED)**		A51	**GND (FIXED)**	
B52	–	–	A52	–	–
B53	–	–	A53	–	–
B54	GPO_1	Input / Output	A54	GPI_0	Input / Output
B55	–	–	A55	–	–
B56	–	–	A56	–	–
B57	GPO_2	Input / Output	A57	**GND**	
B58	–	–	A58	–	–
B59	–	–	A59	–	–
B60	**GND (FIXED)**		A60	**GND (FIXED)**	
B61	PCIE_RX2+	Input	A61	PCIE_TX2+	Output
B62	PCIE_RX2-	Input	A62	PCIE_TX2-	Output
B63	GPO_3	Input / Output	A63	GPI_1	Input / Output
B64	PCIE_RX1+	Input	A64	PCIE_TX1+	Output
B65	PCIE_RX1-	Input	A65	PCIE_TX1-	Output
B66	WAKE0#	Input	A66	**GND**	
B67	WAKE1#	Input	A67	GPI_2	Input / Output
B68	PCIE_RX0+	Input	A68	PCIE_TX0+	Output
B69	PCIE_RX0-	Input	A69	PCIE_TX0-	Output

XS1: COM Express Connector Socket 220-pin Type I (3-6318490-6, TYCO)					
Contact #	Purpose	Configuration	Contact #	Purpose	Configuration
B70	**GND (FIXED)**		A70	**GND (FIXED)**	
B71	SDVO_RED+	Output	A71	LVDS_A0+	Output
B72	SDVO_RED-	Output	A72	LVDS_A0-	Output
B73	SDVO_GREEN+	Output	A73	LVDS_A1+	Output
B74	SDVO_GREEN-	Output	A74	LVDS_A1-	Output
B75	SDVO_BLUE+	Output	A75	LVDS_A2+	Output
B76	SDVO_BLUE+	Output	A76	LVDS_A2-	Output
B77	SDVO_INT+	Input	A77	LVDS_VDD_EN	Output
B78	SDVO_INT-	Input	A78	LVDS_A3+	Output
B79	LVDS_BKLT_EN	Output	A79	LVDS_A3-	Output
B80	**GND (FIXED)**		A80	**GND (FIXED)**	
B81	SDVO_CLK+	Output	A81	LVDS_A_CK+	Output
B82	SDVO_CLK-	Output	A82	LVDS_A_CK-	Output
B83	LVDS_BKLT_CTRL	Output	A83	LVDS_I2C_CK	Output
B84	VCC_5V_SBY	Input (power)	A84	LVDS_I2C_DAT	Input / Output
B85	VCC_5V_SBY	Input (power)	A85	GPI_3	Input / Output
B86	VCC_5V_SBY	Input (power)	A86	–	–
B87	VCC_5V_SBY	Input (power)	A87	–	–
B88	BIOS_DIS1#	Input	A88	PCIE0_CK_REF+	Output
B89	–	–	A89	PCIE0_CK_REF-	
B90	**GND (FIXED)**		A90	**GND (FIXED)**	
B91	SDVO_TVCLKIN+	Input	A91	SPI_POWER	Output
B92	SDVO_TVCLKIN-	Input	A92	SPI_MISO	Input
B93	SDVO_FLDSTAL+	Input	A93	GPO_3	Input / Output
B94	SDVO_FLDSTAL-	Input	A94	SPI_CLK	Output
B95	DDC_AUX_SEL	Output	A95	SPI_MOSI	Output
B96	USB_HOST_PRSNT	Input	A96	PP_TPM	Input
B97	SPI_CS#	Output	A97	TYPE10#	Output
B98	SDVO_CTR_CLK	Output	A98	SER0_TX	Output
B99	SDVO_CTRL_DAT	Input / Output	A99	SER0_RX	Input
B100	**GND (FIXED)**		A100	**GND (FIXED)**	
B101	FAN_PWMOUT	Output	A101	SER1_TX	Output
B102	FAN_TACHIN	Input	A102	SER1_RX	Input
B103	SLEEP#	Input	A103	LID#	Input
B104	VCC_12V	Input (power)	A104	VCC_12V	Input (power)
B105	VCC_12V	Input (power)	A105	VCC_12V	Input (power)
B106	VCC_12V	Input (power)	A106	VCC_12V	Input (power)
B107	VCC_12V	Input (power)	A107	VCC_12V	Input (power)

XS1: COM Express Connector Socket 220-pin Type I (3-6318490-6, TYCO)					
Contact #	Purpose	Configuration	Contact #	Purpose	Configuration
B108	VCC_12V	Input (power)	A108	VCC_12V	Input (power)
B109	VCC_12V	Input (power)	A109	VCC_12V	Input (power)
B110	GND (FIXED)		A110	GND (FIXED)	

* SATA1 port is available only in CPB907-02, CPB907-03.

2.8.1 HAD interface (High Definition Audio)

High Definition Audio interface is used for the connection of an external audio codec on the carrier- board.

Signal	Type and level	Description
AC/HDA_RST#	Output, CMOS 3.3 V	Reset signal for external audio codec.
AC/HDA_SYNC	Output, CMOS 3.3 V	Synchronizing signal for external audio codec.
AC/HDA_BITCLK	Input / Output, CMOS 3.3 V	Clock signal of external audio codec
AC/HDA_SDOUT	Output, CMOS 3.3 V	Data signal for external audio codec.
AC/HDA_SDIN0	Input / Output, CMOS 3.3 V	Data signal from the first audio codec.
AC/HDA_SDIN1	Input / Output, CMOS 3.3 V	Data signal from the second audio codec.
AC/HDA_SDIN2	Input / Output, CMOS 3.3 V	Data signal from the third audio codec. * not used in CPB907

2.8.2 Gigabit Ethernet interface

Intended for connection of devices supporting 10/100/1000 Mb Ethernet. Transformer should be located on the carrier-board.

<table>
<tr><th>Signal</th><th>Type</th><th>Description</th></tr>
<tr><td>GBE0_MDI3-,
GBE0_MDI3+
GBE0_MDI2-,
GBE0_MDI2+
GBE0_MDI1-,
GBE0_MDI1+
GBE0_MDI0-,
GBE0_MDI0+</td><td>Input / Output
Analog 3.3 V</td><td>Data signals (differential couples) of Gbit Ethernet interface. Operation in 1000 / 100 / 10 Mb/s modes is possible. DEpending on the mode, couple purpose is changing:
<table>
<tr><th></th><th>1000BASE-T</th><th>100BASE-T</th><th>10BASE-T</th></tr>
<tr><td>GBE0_MDI0 +/-</td><td>B1_DA+/-</td><td>TX+/-</td><td>TX+/-</td></tr>
<tr><td>GBE0_MDI1 +/-</td><td>B1_DB+/-</td><td>RX+/-</td><td>RX+/-</td></tr>
<tr><td>GBE0_MDI2 +/-</td><td>B1_DC+/-</td><td>–</td><td>–</td></tr>
<tr><td>GBE0_MDI3 +/-</td><td>B1_DD+/-</td><td>–</td><td>–</td></tr>
</table></td></tr>
<tr><td>GBE0_ACT#</td><td>Output 3.3 V (Bare collector)</td><td>Activity indication signal</td></tr>
<tr><td>GBE0_LINK#</td><td>Output 3.3 V (Bare connector)</td><td>Connection setup signal</td></tr>
</table>

Signal	Type	Description
GBE0_CTREF	Reference voltage, GND	Reference voltage signal for midpoint of external electric transformer on the carrier-board.
GBE0_LINK100#	Output, 3.3 V (Open collector)	Connection setup signal 100 Mb/s * not used in CPB907
GBE0_LINK1000#	Output, 3.3 V (Open collector)	Connection setup signal 1000 Mb/s * not used in CPB907

2.8.3. SATA ports

SATA interface is intended for the connection of SATA I and SATA II external drives.

Signal	Type and level	Description
SATA0_TX+ SATA0_TX-	Output, 1.2 V (SATA)	Data transfer signal (differential couple) of SATA0 interface. Alternating current coupling.
SATA0_RX+ SATA0_RX-	Input, 1.2 V (SATA)	Data receipt signal (differential couple) of SATA0 interface. Alternating current coupling.
SATA1_TX+ SATA1_TX-	Output, 1.2 V (SATA)	Data transfer signal (differential couple) of SATA1 interface. Alternating current coupling. * available only in CPB907-02, CPB907-03
SATA1_RX+ SATA1_RX-	Input, 1.2 V (SATA)	Data receipt signal (differential couple) of SATA1 interface. Alternating current coupling. * available only in CPB907-02, CPB907-03
SATA_ACT#	Input/Output, CMOS 3.3 V	Signal of SATA ports activity indication.

2.8.4. PCIe ports

PCIe interface is designed for the connection of external PCIe-compatible devices.

Signal	Type and level	Description
PCIE_TX0+ PCIE_TX0-	Output, 1.2 V (PCIe)	Data transfer signal (differential couple) of PCIE0 interface. Alternating current coupling.
PCIE_RX0+ PCIE_RX0-	Input, 1.2 V (PCIe)	Data receipt signal (differential couple) of PCIE0 interface. Alternating current coupling..
PCIE_TX1+ PCIE_TX1-	Output, 1.2 V (PCIe)	Data transfer signal (differential couple) of PCIE1 interface. Alternating current coupling.
PCIE_RX1+ PCIE_RX1-	Input, 1.2 V (PCIe)	Data receipt signal (differential couple) of PCIE1 interface. Alternating current coupling.
PCIE_TX2+ PCIE_TX2-	Output, 1.2 V (PCIe)	Data transfer signal (differential couple) of PCIE2 interface. Alternating current coupling.
PCIE_RX2+ PCIE_RX2-	Input, 1.2 V (PCIe)	Data receipt signal (differential couple) of PCIE2 interface. Alternating current coupling.
PCIE_CLK_REF+ PCIE_CLK_REF-	Output, 1.2 V (PCIe)	Reference clock signal for all external PCIe devices.
EXCD0_CPPE#	Input, CMOS 3.3 V	Signal of availability of PCIe-compatible card (PCI Express capable card request).
EXCD1_CPPE#	Input, CMOS 3.3 V	Signal of availability of PCIe-compatible card (PCI Express capable card request).

Signal	Type and level	Description
EXCD0_PERST#	Output, CMOS 3.3 V	Reset signal for PCIe-compatible card.
EXCD1_ PERST #	Output, CMOS 3.3 V	Reset signal for PCIe-compatible card.

* Signals of PCIE3 port (PCIE_TX3+||PCIE_TX3-, PCIE_RX3+||PCIE_RX3-) are not used in CPB907.

2.8.5. USB ports

SATA is intended for connection of SATA I and SATA II external drives.

Signal	Type and level	Description
USB0+ USB0-	Input/Output, CMOS 3.3 V	USB0 port (USB 2.0 Host), data receipt and transfer signal (differential couple).
USB1+ USB1-	Input/Output, CMOS 3.3 V	USB1 port (USB 2.0 Host), data receipt and transfer signal (differential couple).
USB2+ USB2-	Input/Output, CMOS 3.3 V	USB2 port (USB 2.0 Host), data receipt and transfer signal (differential couple).
USB3+ USB3-	Input/Output, CMOS 3.3 V	USB3 port (USB 2.0 Host), data receipt and transfer signal (differential couple).
USB4+ USB4-	Input/Output, CMOS 3.3 V	USB4 port (USB 2.0 Host), data receipt and transfer signal (differential couple).
USB5+ USB5-	Input/Output, CMOS 3.3 V	USB5 port (USB 2.0 Host), data receipt and transfer signal (differential couple).
USB7+ USB7-	Input/Output, CMOS 3.3 V	USB7 port (USB 2.0 Host), data receipt and transfer signal (differential couple).

* Signals of USB6 port (differential couples USB6+ || USB6-) are not used in CPB907 module.

2.8.6. LVDS port

LVDS interface is intended for the connection of external flat panels. Support of 18 / 24 bit modes, control of panel illumination and power supply.

Signal	Type and level	Description
LVDS[3:0]+ LVDS[3:0]-	Output, LVDS (1.25 V)	LVDS differential couples
LVDS_CK+ LVDS_CK-	Output, LVDS (1.25 V)	LVDS differential reference clock signal
LVDS_VDD_EN	Output, 3.3 V	Signal of panel power-up
LVDS_BKLT_EN	Output, 3.3 V	Signal for switching-on of panel illumination
LVDS_BKLT_CTRL	Output, 3.3 V	Signal of panel illumination brightness control
LVDS_I2C_CK	Input/Output, 3.3 V (Open collector)	Line of I2C clock signal for the panel
LVDS_I2C_DAT	Input/Output, 3.3 V (Open collector)	Line of I2C data for the panel

2.8.7 LPC Bus

The LPC bus is intended for connection of external devices on the carrier-board (e.g. LPC Super-IO for extension of the range of I/O interfaces).

Signal	Type and level	Description
LPC_AD[3:0]	Input/Output, CMOS 3.3 V	Multiplexed address/data LPC bus
LPC_FRAME#	Output, CMOS 3.3 V	Signal of cycle start of exchange over the LPC bus.
LPC_SERIRQ	Input/Output, CMOS 3.3 V	Serial interrupt line of LPC bus. *
LPC_CLK	Output, CMOS 3.3 V	Reference clock signal for LPC bus, rated frequency 33 MHz.

* Signals of LPC_DRQ[1:0]# are not used in CPB907 (direct access mode is not supported by LPC bus controller).

2.8.8. SPI port

SPI interface is intended for the connection of flash memory microchips of 2 MB on the carrier-board for loading of BIOS.

Signal	Type and level	Description
SPI_CS#	Output, CMOS 3.3 V	Enabling signal (Chip Select) for SPI microchip of flash memory on the carrier-board.
SPI_MISO	Input, CMOS 3.3 V	Data signal for SPI microchip of flash memory on the carrier-board.
SPI_MOSI	Output, CMOS 3.3 V	Data signal for SPI microchip of flash memory on the carrier-board.
SPI_CLK	Output, CMOS 3.3 V	Reference clock signal for SPI microchip of flash memory on the carrier-board.
SPI_POWER	Output, CMOS 3.3 V	Power supply voltage of 3.3V for SPI microchip of flash memory on the carrier-board. Rated current – 100 mA.
BIOS_DIS0# BIOS_DIS1#	Input, CMOS 3.3 V	Selection of BIOS booting sources. When there are installed logical levels BIOS_DIS1# = '0' and BIOS_DIS0# = '1' BIOS boot is carried out from the SPI flash memory, installed onto the carrier-board, in other cases, BIOS is booted from the CPB907 module.

2.8.9. DDI (SDVO) port

A serial digital video interface (SDVO) for the connection of SDVO-VGA, SDVO-LVDS, SDVO-HDMI/DVI on the carrier-board is used as DDI (Digital Display Interface) port.

Signal	Type and level	Description
SDVO_RED+ SDVO_RED-	Output, 1.2 V (PCIe)	Differential serial digital video signal (red).
SDVO_GREEN+ SDVO_GREEN-	Output, 1.2 V (PCIe)	Differential serial digital video signal (green).
SDVO_BLUE+ SDVO_BLUE+	Output, 1.2 V (PCIe)	Differential serial digital video signal (blue).

Signal	Type and level	Description
SDVO_CLK+ SDVO_CLK-	Output, 1.2 V (PCIe)	Differential clock signal of serial digital video interface.
SDVO_INT+ SDVO_INT-	Input, 1.2 V (PCIe)	Differential interrupt input of serial digital video interface.
SDVO_TVCLKIN+ SDVO_TVCLKIN-	Input, 1.2 V (PCIe)	Differential input of TVOUT synchronization clock signal.
SDVO_FLDSTAL+ SDVO_FLDSTAL-	Input, 1.2 V (PCIe)	Field Stall differential input of serial digital video interface
SDVO_CTR_CLK	Input/Output, 2.5 V (Open collector)	Line of I2C clock signal for setting up the connected SDVO devices.
SDVO_CTR_CLK	Input/Output, 2.5 V (Open collector)	Line of I2C data for setting up the connected SDVO devices.
DDC_AUX_SEL	Input, CMOS 3.3 V	Control of the purpose of outputs SDVO_CTR_CLK/ SDVO_CTR_CLK of COM Express connector. In CPB907 module, the line status is ignored, since serial digital video interface SDVO is used (in this case the purpose of SDVO_CTR_CLK/ SDVO_CTR_CLK is defined by hardware).

2.8.10. I2C Port

I2C port is intended for connection of the devices located on the carrier-board, supporting exchange rate of 100/400 kHz. Maximum capacitive load on each line should not exceed 100 pF. Pull-up resistors of 2.2 kOhm are located on CPB907.

Signal	Type and level	Description
I2C_CK	Input/Output, 3.3 V (Open collector)	Clock signal of I2C interface.
I2C_DAT	Input/Output, 3.3 V (Open collector)	Data signal of I2C interface.

2.8.11. SER0, SER1 serial ports

Asynchronous serial ports SER0, SER1 (compatible with the version 16550 PC AT UART). In addition, SER1 port can be used for output of CAN interface. Transmitter/receiver units should be located on the carrier-board.

Signal	Type and level	Description
SER0_TX	Output, CMOS 3.3 V	Data transfer signal of SER0 serial port.
SER0_RX	Input, CMOS 3.3 V	Data receipt signal of SER0 serial port.
SER1_TX	Output, CMOS 3.3 V	Data transfer signal of SER1 serial port (UART / CAN).
SER1_RX	Input, CMOS 3.3 V	Data receipt signal of SER1 serial port (UART / CAN).

2.8.12. SMBus port

SM Bus port is intended for such system functions as e.g. reading system parameters, control of peripheral devices. Maximum capacitive load on each SM Bus line should not exceed 100 pF.

Signal	Type and level	Description
SMB_CK	Input/Output, 3.3 V (Open collector)	Clock signal of I2C interface.
SMB_DAT	Input/Output, 3.3 V (Open collector)	Data signal of I2C interface.
SMB_ALERT#	Input, CMOS 3.3 V	Input signal of SM Bus with an active low level, used for generation of system interrupt SMI or device wake-up from the standby mode S3 into an active state

2.8.13. GPIO/SDIO port

GPIO port is intended for the output of eight I/O digital signals.
In addition, GPIO lines can be used for the routing of SDIO interface to the carrier-board. The purpose of the port is changed by switching, this can be carried put in the BIOS Setup settings.

Signal	Type and level	Description
GPI0/SD_DATA0	Input/Output, CMOS 3.3 V	Signal GPI0 / Data signal SD_DATA0.
GPI1/SD_DATA1	Input/Output, CMOS 3.3 V	Signal GPI1 / Data signal SD_DATA1.
GPI0/SD_DATA2	Input/Output, CMOS 3.3 V	Signal GPI2 / Data signal SD_DATA2.
GPI1/SD_DATA3	Input/Output, CMOS 3.3 V	Signal GPI3 / Data signal SD_DATA3.
GPO0	Output, CMOS 3.3 V	Signal GPO0 / Clock signal SD_CLK.
GPO1	Output, CMOS 3.3 V	GPO1 signal / Control signal SD_CMD.
GPO2	Input, CMOS 3.3 V	Signal GPO2 / Write protection signal SD_WP.
GPO3	Input, CMOS 3.3 V	Signal GPO3 / Card present signal SD_CD#

2.8.14. System signals and power supply

Asynchronous serial ports SER0, SER1 (compatible with the version 16550 PC AT UART). In addition, SER1 port can be used for the output of CAN interface. Transmitter/receiver units should be located on the carrier-board.

Signal	Type and level	Description
PWRBTN#	Input, CMOS 3.3 V	Power on signal. Reverse front (changeover from the high level down to the low level) causes the "Power Button" event within the system (changeover from S3 to S0 mode, from S0 to S3 mode). Long-time holding down of PWRBTN# at the low level (for more than 6 seconds) leads to the changeover of the system from S0 to S4/S5 mode.
SYS_RESET#	Input, CMOS 3.3 V	Hardware reset signal of CPB907.
CB_RESET#	Output, CMOS 3.3 V	Hardware reset signal of CPB907. Active low level
PWR_OK	Input, CMOS 3.3 V	"Power OK" signal from the power supply source. High level demonstrates entering into operating mode of power supply voltages used. The signal can also be used for the delay of automatic start of the system after switching on the power supply.
SUS_STAT#	Output, CMOS 3.3 V	Signal of indication of transferring to the standby mode.
SUS_S3#	Output, CMOS 3.3 V	Signal of indication of S3 condition (Suspend to RAM).
SUS_S4#	Output, CMOS 3.3 V	Signal of indication of S4 condition (Suspend to Disk).
SUS_S5#	Output, CMOS 3.3 V	Signal of indication of S5 condition (Soft Off state).
WAKE0#	Input, CMOS 3.3 V	Active low signal of system wake-up from PCIe devices on the carrier-board
WAKE1#	Input, CMOS 3.3 V	General purpose active low signal of system wake-up
BATLOW#	Input, CMOS 3.3 V	Active low signal of external battery low level.
LID#	Input, 3.3 V (Open collector)	Input signal from carrier-board. Active low level transfers the system into the standby mode S0→S3 or brings the system from standby mode S3→S0.
SLEEP#	Input, 3.3 V (Open collector)	Input signal from the carrier-board. Active low level turns system to the standby mode S0→S3 or brings the system from the standby mode S3→S0.
THRM#	Input, CMOS 3.3 V	Input signal from temperature sensor, located on the carrier-board. Indication of excessive heating.
THRMTRIP#	Output, CMOS 3.3 V	Signal of input indication of CPB907 in the emergency switch-off of the power supply due to the excessive heating.
SPKR	Output, CMOS 3.3 V	Signal of PC buzzer control. For control of PC-buzzer on the carrier-board it is required to install the driver (e.g. bipolar transistor).
WDT	Output, CMOS 3.3 V	Signal of indication of watchdog timer activation
FAN_PWMOUT	Output, 3.3 V (Open collector)	PWM signal for control of external fan rotation speed. It is required to install the driver on the carrier-board (e.g. field-effect transistor).

Signal	Type and level	Description
FAN_TACHIN	Input, 3.3 V (Open collector)	Tachometer signal from the fan of the carrier-board.
TPM_PP	Input, CMOS 3.3 V	Signal of availability of TPM (Trusted Platform Module) module within the system. Active high level.

SECTION 3
Intended use of CPB907

3. Intended use of CPB907

The module can be installed on the carrier-board with a compatible COM Express Type 10 connector and availability of lead holes.

Attention!

The module contains sensing elements. Installation, removal of the modules, connection to the connectors when the power is on and a static charge of your hands can lead to it breakdown.

Attention!

When installing, it is required to observe the correct orientation of the module's connectors relative to the carrier board connectors.

Attention!

To ensure the above mechanical and electrical characteristics, it is necessary to install fasteners, supplied together with the module. Distortions of the module in the mating part of the connector on the carrier-board are not allowed and could lead to damages of the both CPB907 CPU module and carrier-board.

3.1. Installation of module switches

For hardware configuration of the module, a group of switches will be used.
A general description of such switches is given in the table below. The switches are arranged so that the presence of the heat-distribution plate or heat-sink does not prevent from installation or removal of switches.

Table 3-1: Purpose of switches for module configuration

Switches	Description
X1 [1-2]	Reset of CMOS settings. In case of the closed jumper, BIOS settings and time/data are reset.
X2 [1-2]	In case of the closed jumper, the module will be started (changeover to the S0 mode) after switching on of power supply. If the jumper is opened, the module is started (changeover to the S0 mode) during the closure of PWRBTN# line of COM Express connector onto the ground (GND circuit). After module's changeover in to the S4/S5 mode for starting the module, it is required to close the PWRBTN# line of the COM Express connector to the ground (GND circuit).

3.2. Basic Input-output system (BIOS)

Using the BIOS Setup Utility software, it is possible to change various parameters of basic Input-output system (BIOS), as well as control special operation modes of the module. For editing BIOS parameters, system menu is used.
In order to enter BIOS Setup, while loading the system, during the POST (Power On Self Test) it is required to push “DEL” or “F2” button on the keyboard. Example of the screen during the run of the POST procedure is shown in figure 3-1.

Fig. 3-1: Screen during module booting (POST)

Using the BIOS Setup Utility program, it is possible to change parameters of BIOS (Basic Input Output System) and control special operation modes of the module. This program uses menu system for introducing changes, as well as for switching on or switching off special functions.
Information fields (highlighted with grey font color) are designed for output of additional information on the module and/or module settings and can’t be changed by user.

Main

This menu tab contains description of a version of BIOS modules and information on the installed RAM. There are also two menu items responsible for setting a current time and date, setting interface language as well as a sub-item, which contain a detailed information on the platform.

Fig. 3-2: Screen of "Main" menu

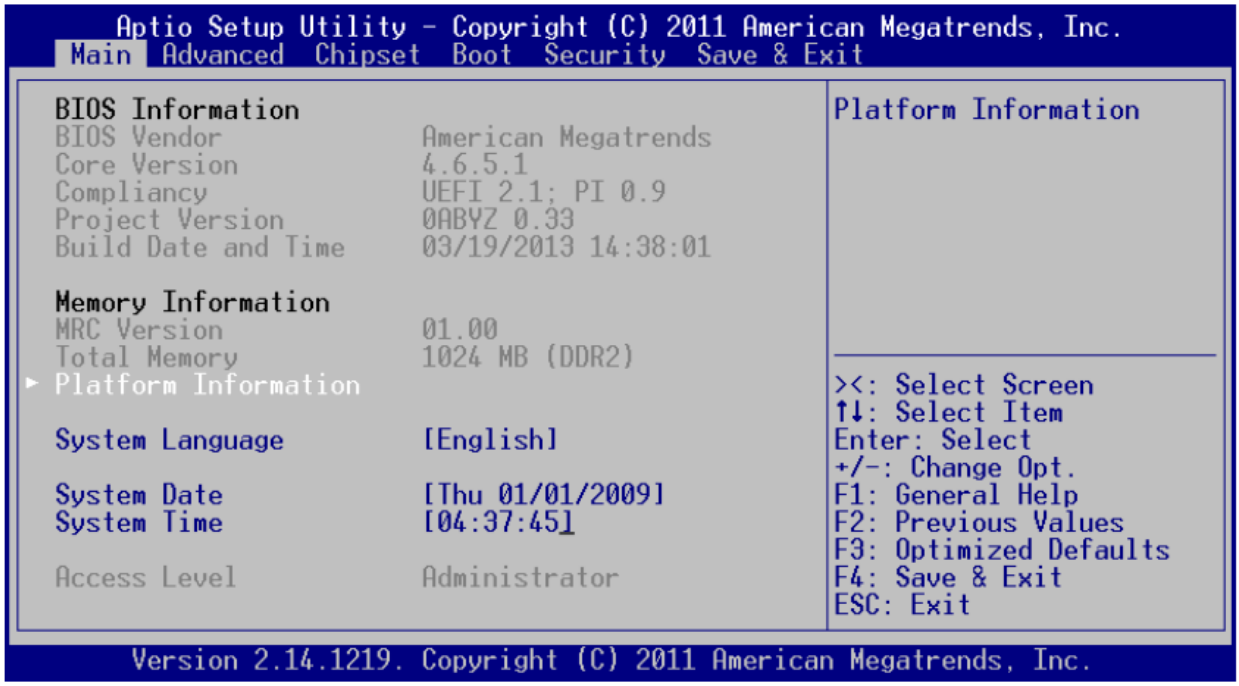


Table 3-2: Description of "Main" menu

Menu item	Description
BIOS Information	Versions of BIOS modules, build data and project-related information.
Memory Information	Version of memory initialization module, size of the installed RAM.
Platform Information	Information on CPU version
System Language	Interface language (only English is available)
System Date	Current date
System Time	Current time

Advanced (additional settings)

This menu tab contains items, which are responsible for operation of PCI bus, CPU, SD and SUPER-IO controllers, console I/O and USB devices.

Fig. 3-3: Screen of "Advanced" menu

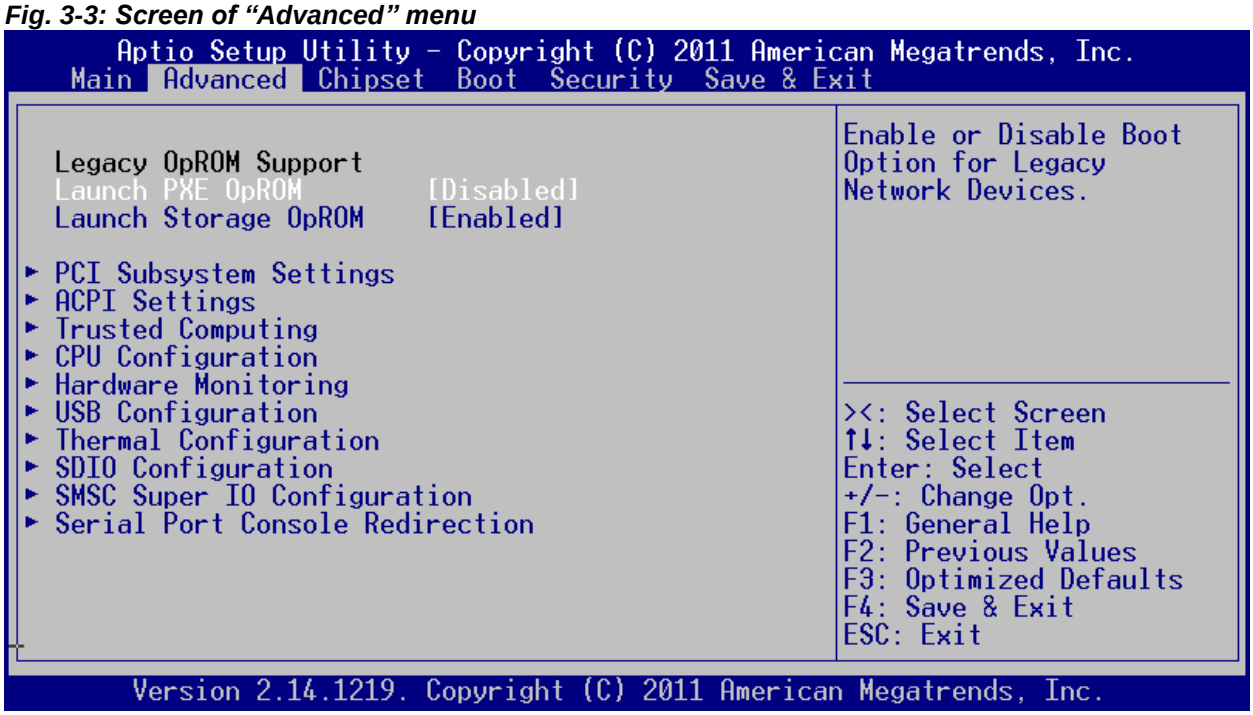


Table 3-3: Description of "Advanced" menu

Menu item	Description
Legacy OpROM Support	Adjustment of support of the Legacy Optional ROM for network interface cards and carriers
PCI Subsystem Settings	Configuration of PCI bus operation
ACPI Settings	ACPI
CPU Configuration	Additional settings and CPU information.
Hardware Monitoring	Information of temperature and voltage sensors, information on the availability of optional devices on SMBus
USB Configuration	Information and additional bus and USB settings
Thermal Configuration	Settings of active and passive CPU cooling policies
SDIO Configuration	Setting of controllers and SD devices
SMSC Super IO Configuration	Configuration of COM and LPT ports, implemented via Super IO
Serial Port Console Redirection	Setting an access to the console via Serial Port

PCI Subsystem Settings

This menu tab demonstrates items, responsible for operation of the PCI bus.

Fig. 3-4: Screen of "PCI Subsystem Settings" menu

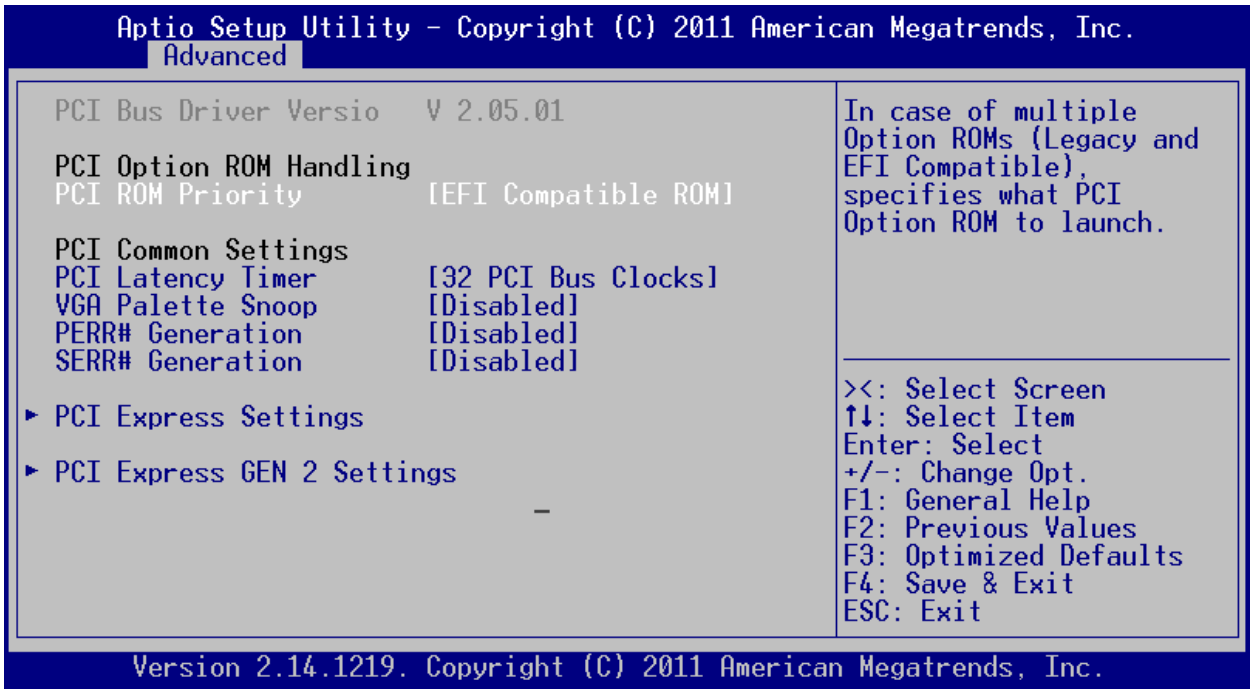


Table 3-4: Description of "PCI Subsystem Settings" menu

Menu item	Description
PCI ROM Priority	Priority for loading of PCI Option ROM – EFI Compatible or Legacy
PCI Latency Timer	Maximum number of PCI bus cycles, within which a devices connected to this bus can hold it busy, transferring data
VGA Palette Snoop	Adjustment of VGA graphic palette of the graphics card on PCI

ACPI Settings

This menu tab contains items responsible for ACPI support.

Fig. 3-5: Screen of "ACPI Settings" menu

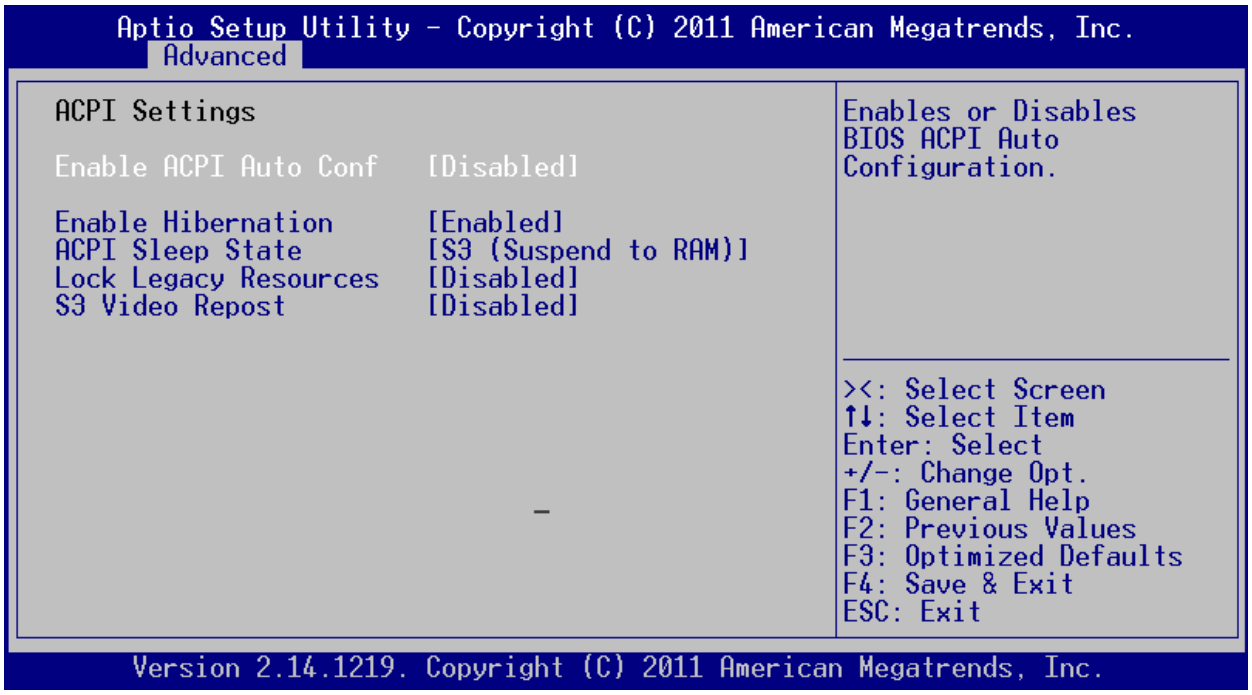


Table 3-5: Description of "ACPI Settings" screen

Menu item	Description
Enable ACPI Auto Conf	Enabling ACPI automatic configuration
Enable Hibernation	Enabling hibernation
ACPI Sleep State	ACPI Sleep mode
Lock Legacy Resources	Locking Legacy resources
S3 Video Repost	Defines whether it is necessary to newly initialize the graphics card when exiting the Suspend to RAM electrical standby mode.

CPU Configuration

This menu tab contains additional information on the installed CPU, bus frequency, Cache-memory size, number of cores and additional settings.

Fig. 3-6: Screen of "CPU Configuration" menu

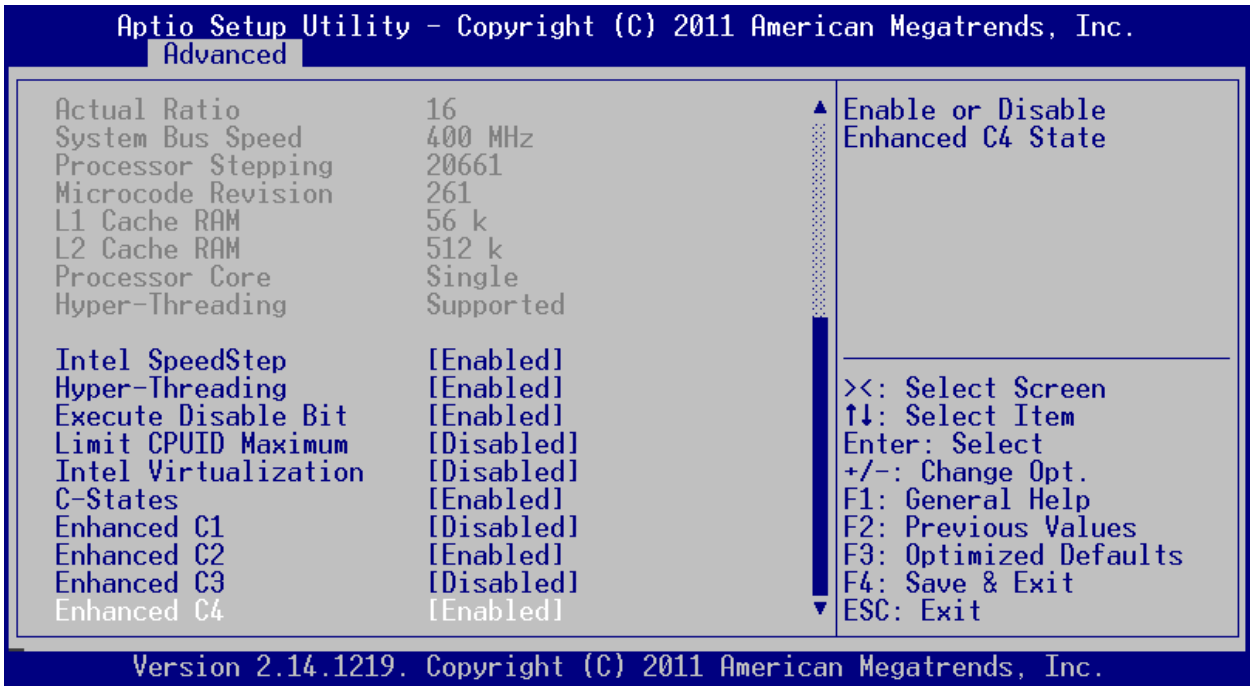


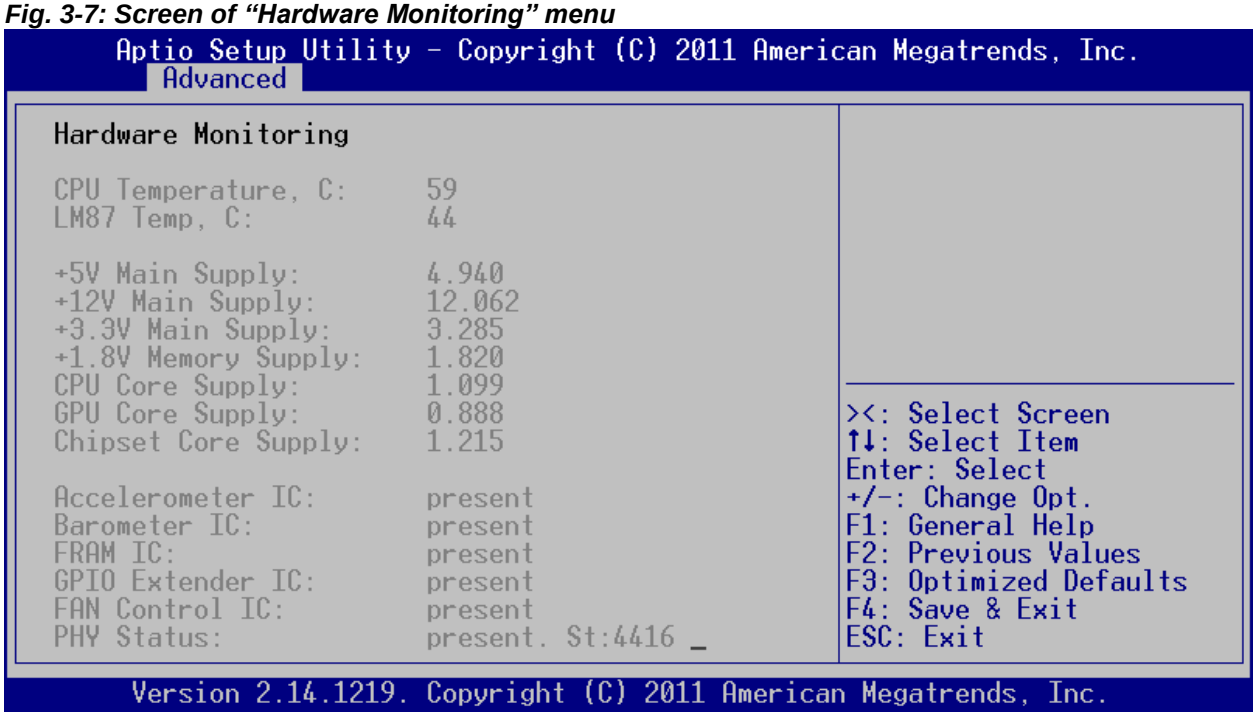
Table 3-6: Description of "CPU Configuration" screen

Menu item	Description
Intel SpeedStep	Automatic reduction in frequency and power supply voltage of CPU in case of a downtime or small load, in order to lower energy consumption
Hyper-Threading	Activation of Hyper-Threading mode
Execute Disable Bit	Use of Execute Disable Bit
Limit CPUID Maximum	Limiting CPUID
Intel Virtualization	Actuation of Intel Virtualization
C-States	This option determines whether the CPU will be switched to the sleep mode when module is switched to the energy efficiency mode.
Enhanced C1	Support of the Enhanced C1 mode
Enhanced C2	Support of the Enhanced C2 mode
Enhanced C3	Support of the Enhanced C3 mode
Enhanced C4	Support of the Enhanced C4 mode

Hardware Monitoring

This menu tab contains information received from temperature and voltage sensors, as well as presence of optional integrated circuits on SMBus.

Fig. 3-7: Screen of "Hardware Monitoring" menu



USB Configuration

This menu tab contains additional information on the connected USB devices and some USB settings.

Fig. 3-8: Screen of "USB Configuration" menu

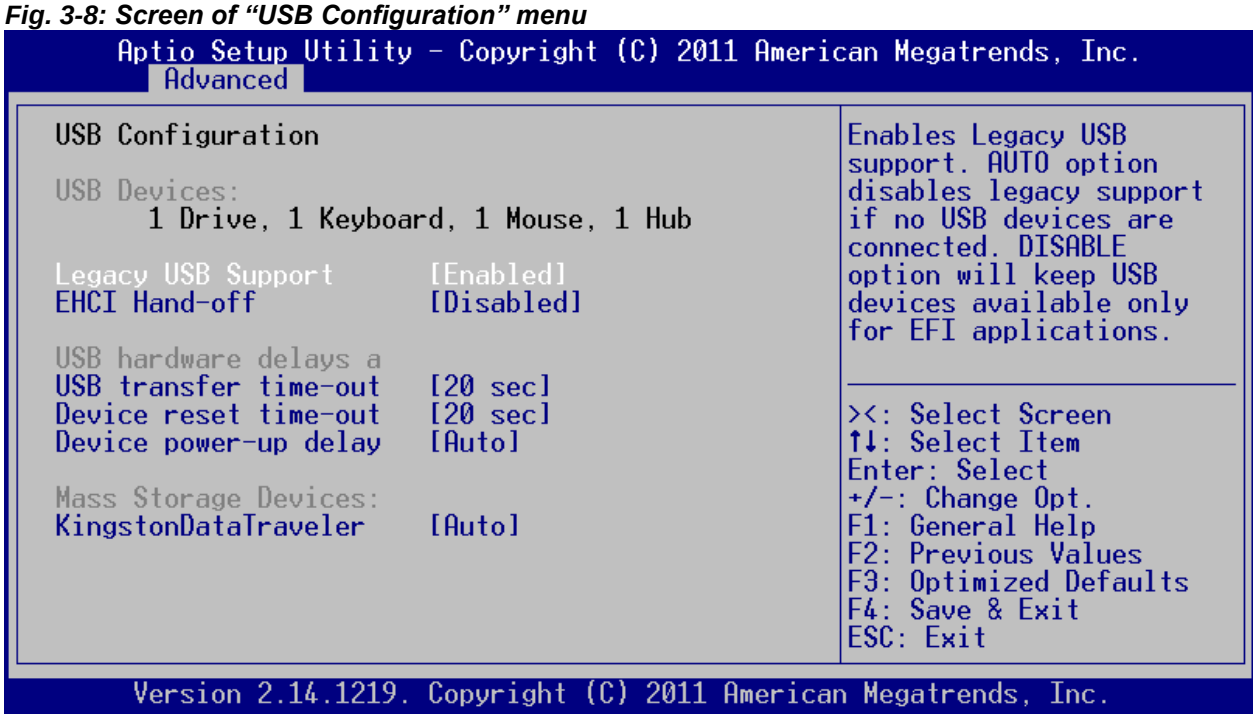


Table 3-7: Description of "USB Configuration" screen

Menu item	Description
USB Devices	List of connected devices
Legacy USB Support	Support of Legacy USB
EHCI Hand-off	This option is responsible for the mechanism of transfer of ECHI interface control of USB 2.0 controller from device to device.
USB transfer time-out	Data transfer time-out
Device reset time-out	Reset time-out
Device power-up delay	Maximum power-up delay
Mass Storage Devices	Confirmation of simulation type for each device

Thermal Configuration

This menu tab contains thermal mode settings of CPU operation.

Fig. 3-9: Screen of "Thermal Configuration" menu

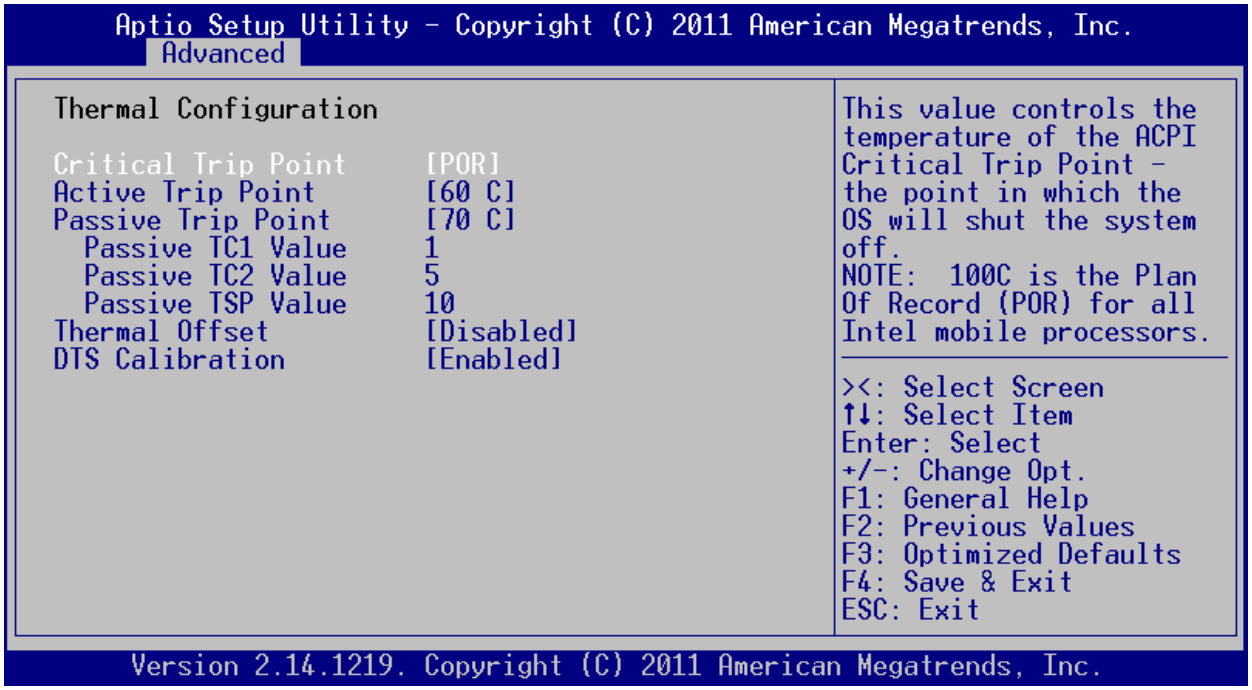


Table 3-8: Description of "Thermal Configuration" screen

Menu item	Description
Critical Trip Point	CPU temperature, at which an automatic emergency shutdown is carried out
Active Trip Point	CPU temperature at which active cooling device is switched on
Passive Trip Point	CPU temperature at which passive cooling mode is switched on
Passive TC1 Value	
Passive TC2 Value	
Passive TSP Value	
Thermal Offset	
DTS Calibration	

SDIO Configuration

This menu tab contains settings of SD controller and connected devices.

Fig. 3-10: Screen of "SDIO Configuration" menu

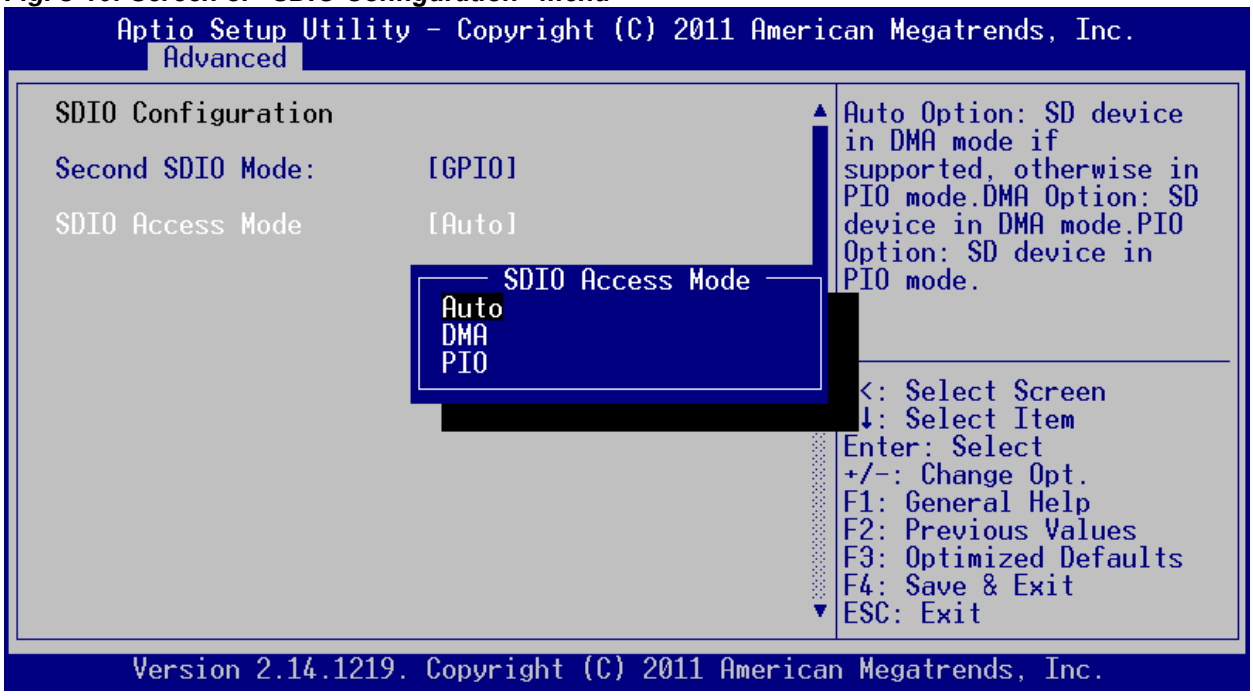


Table 3-9: Description of "SDIO Configuration" menu

Menu item	Description
Second SDIO Mode	Mode of output operation switching – additional SDIO or GPIO
SDIO Access Mode	Operation mode of SD controller

SMSC Super IO Configuration

This menu tab contains the settings of Super IO controller and ports, implemented via this controller.

Fig. 3-11: Screen of "SMSC Super IO Configuration" menu

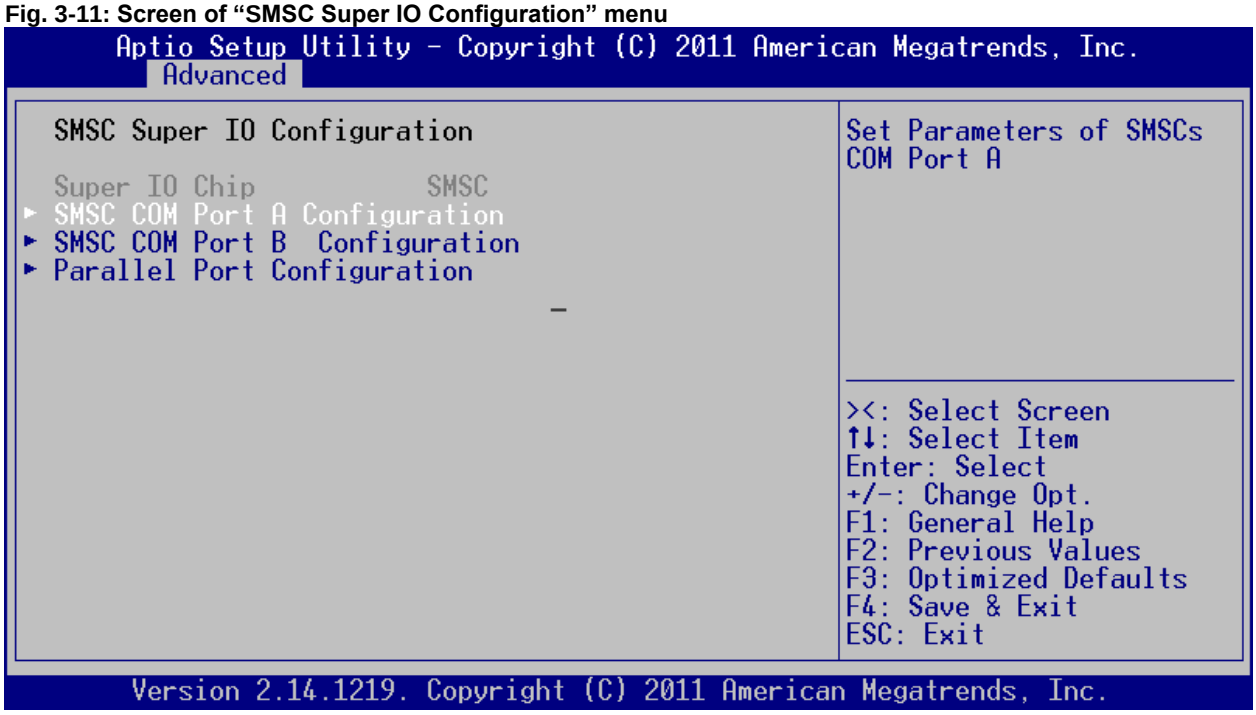


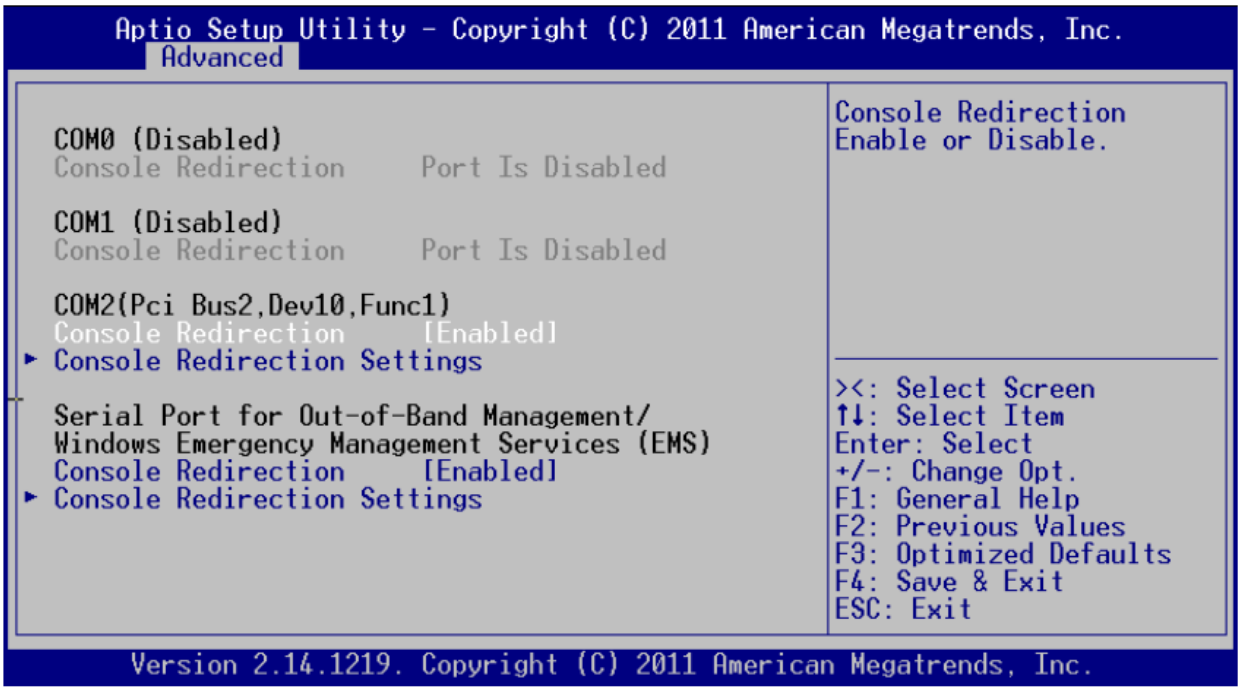
Table 3-10: Description of "SMSC Super IO Configuration" menu

Menu item	Description
Second SDIO Mode	Mode of output operation switching – additional SDIO or GPIO
SMSC COM Port A Configuration	Configuration of the first COM port
SMSC COM Port B Configuration	Configuration of the second COM port
Parallel Port Configuration	Configuration of LPT port

Serial Port Console Redirection

This menu tab contains the settings of console serial ports.

Fig. 3-12: Screen of "Serial Port Console Redirection" menu



Chipset (additional settings)

This menu tab contains additional settings, grouped together by their belonging to module's logic blocks (north and south bridges, I/O ports).

Fig. 3-13: Screen of "Chipset" menu

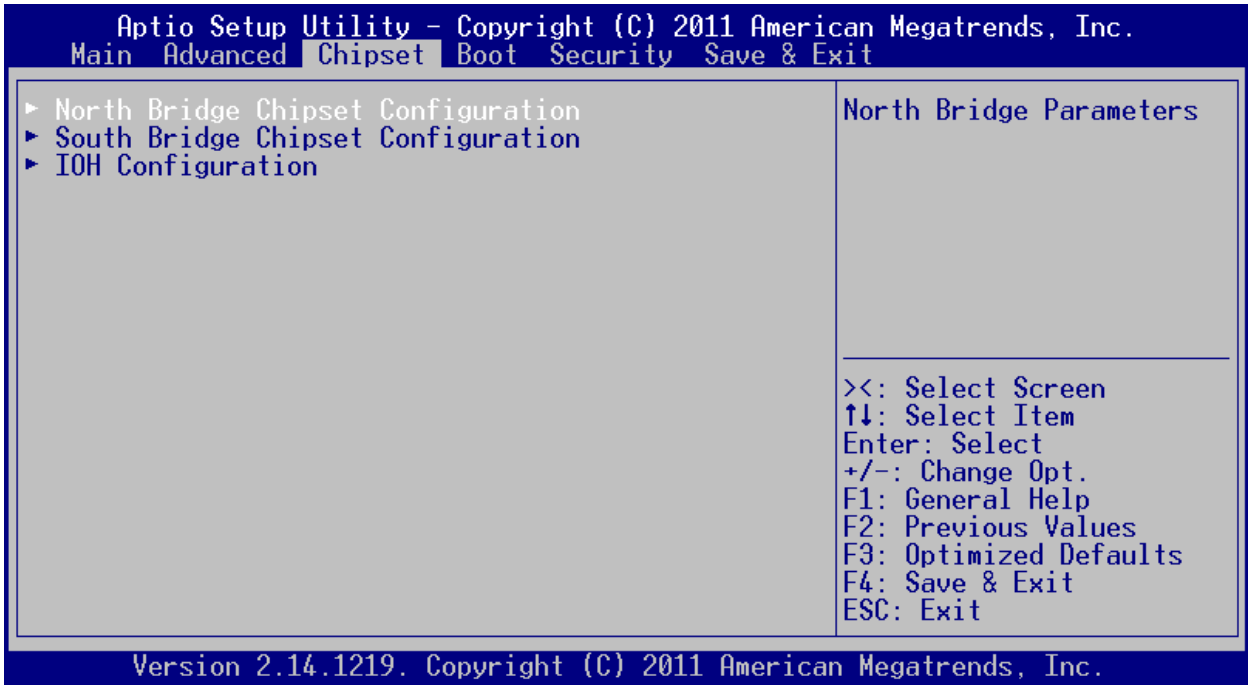


Table 3-11: Description of "Chipset" menu

Menu item	Description
North Bridge Chipset Configuration	Configuration related to the North Bridge
South Bridge Chipset Configuration	Configuration related to the South Bridge
IOH Configuration	Configuration related to I/O ports.

North Bridge Chipset Configuration

The menu tab shows additional configuration related to the North Bridge.

Fig. 3-14: Screen of "North Bridge Chipset Configuration" menu

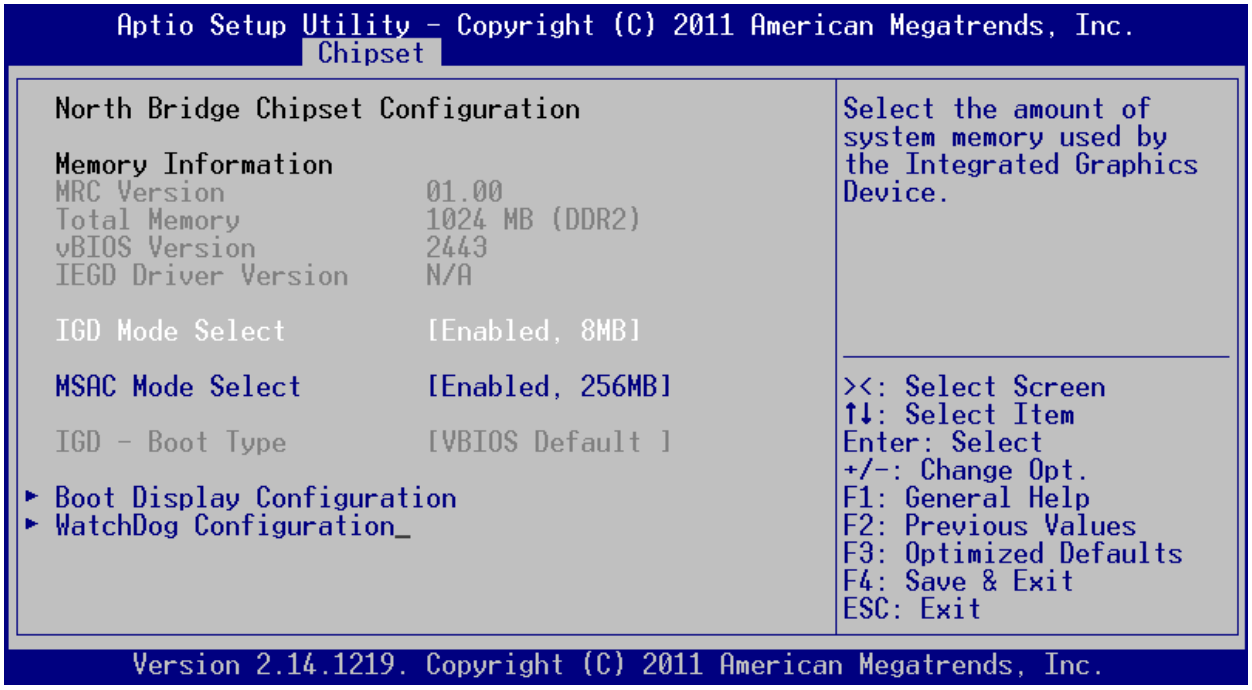


Table 3-12: Description of "North Bridge Chipset Configuration" menu

Menu item	Description
Memory Information	Information on the installed RAM, versions of memory initialization module, video BIOS and IEGD driver
IGD Mode Select	Operation mode and size of dedicated memory for integrated graphics card
MSAC Mode Select	Dedicated memory size for IEGD driver
Boot Display Configuration	Selection and configuration of displaying device, connected at the time of module booting
WatchDog Configuration	WatchDog timer Configuration

South Bridge Chipset Configuration

The menu tab shows additional configuration related to the South Bridge.

Fig. 3-15: Screen of "South Bridge Chipset Configuration" menu

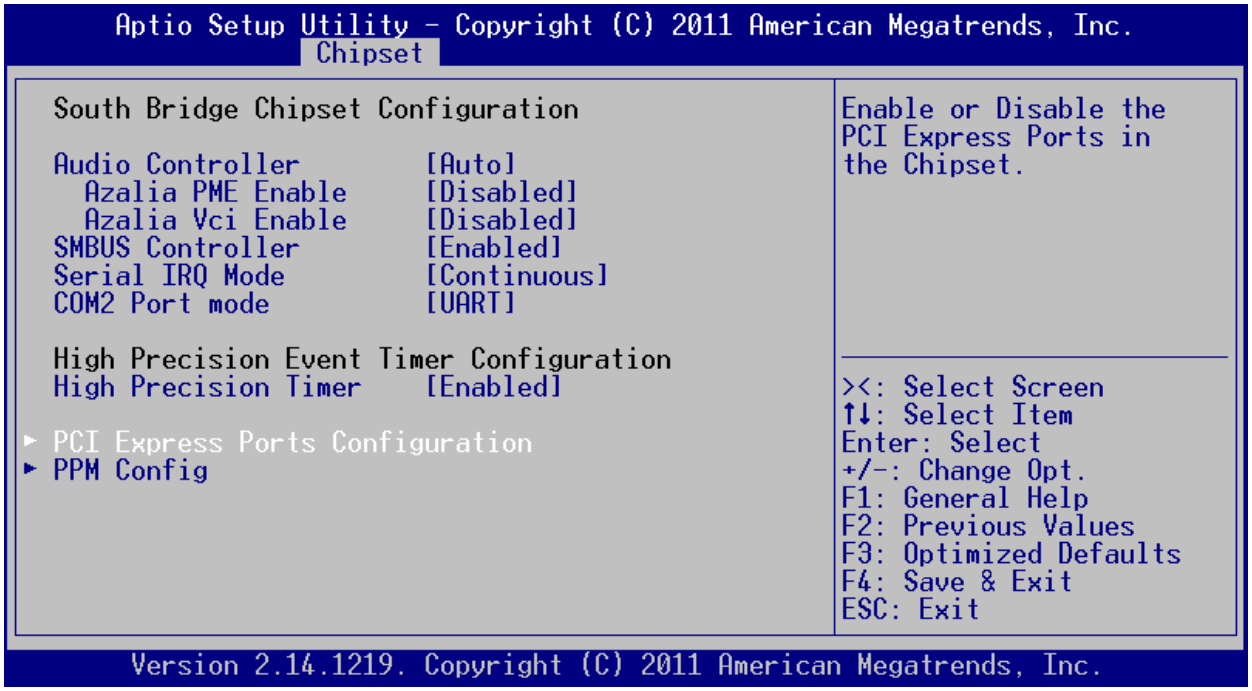


Table 3-13: Description of "South Bridge Chipset Configuration" menu

Menu item	Description
Audio Controller	Audio controller
Azalia PME Enable	
Azalia VCI Enable	
SMBUS Controller	SMBUS Controller
Serial IRQ Mode	
COM2 Port Mode	Mode of port operation COM2 – UART or CAN
High Precision Timer	High Precision Timer
PCI Express Ports Configuration	Additional configuration of PCI Express Ports

IOH Configuration

The menu tab is intended for configuration of AHCI SATA ports, as well as parameters of the system to resume from sleep mode.

Fig. 3-16: Screen of "IOH Configuration" menu

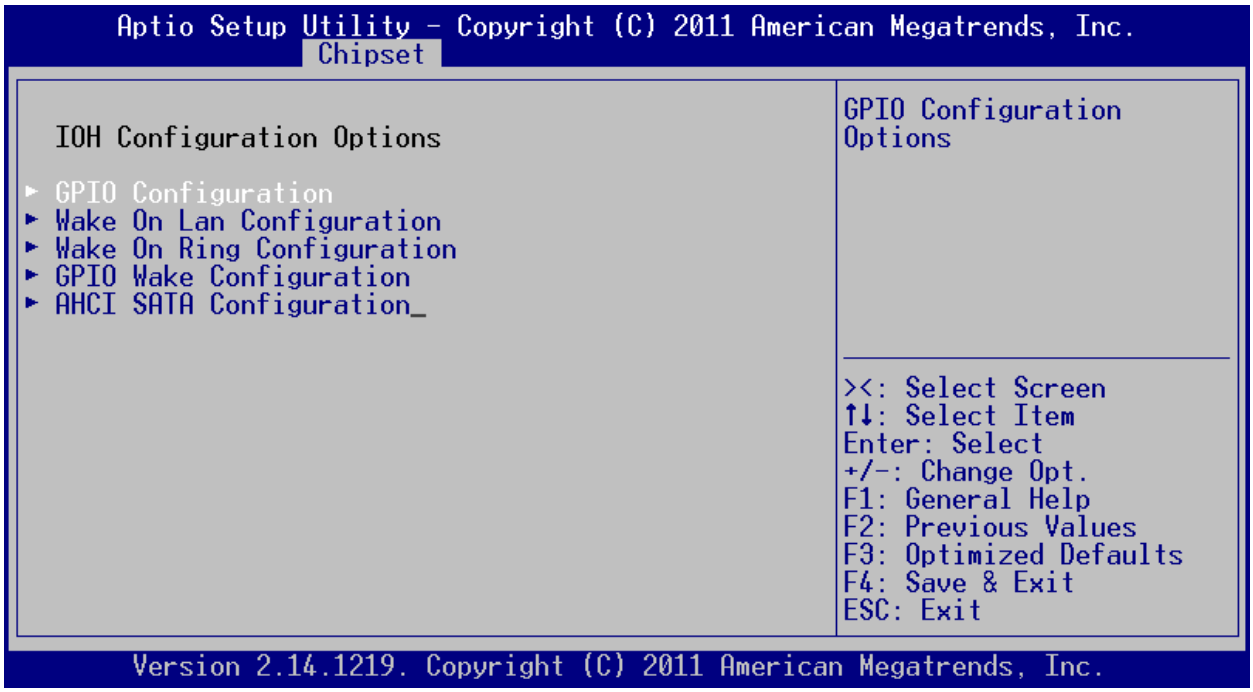


Table 3-14: Description of "IOH Configuration" menu (additional settings)

Menu item	Description
GPIO Configuration	Additional GPIO Configuration
Wake On Lan Configuration	Configuration of "Wake On Lan" (Magic Packet)
Wake On Ring Configuration	Configuration of "Wake On Ring" of serial ports
GPIO Wake Configuration	GPIO Wake Configuration
AHCI SATA Configuration	Configuration of SATA controller ports

Boot

This menu tab contains configuration of booting procedure and boot devices.

Fig. 3-17: Screen of "Boot" menu

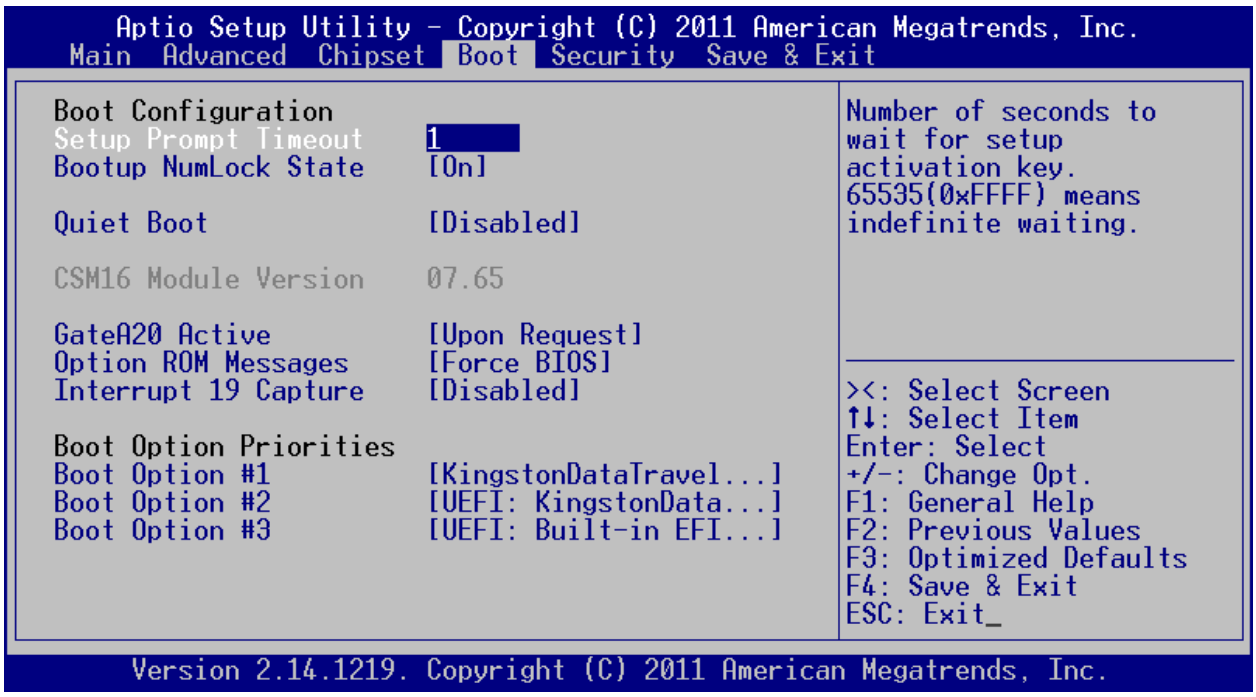


Table 3-15: Description of "Boot" menu

Menu item	Description
Setup Prompt Timeout	Timeout for striking the key for entering BIOS Setup
Bootup NumLock State	NumLock state after POST
Quiet Boot	Quiet boot mode – without output of diagnostic messages
GateA20 Active	Control of A20 address bus shutdown process
Option ROM Messages	Shutting down of messages output from Option ROM
Interrupt 19 Capture	Enables/Disables Interrupt 19 Capture
CSM16 Module Version	Legacy version of CSM16 module
Boot Option Priorities	Boot option priority

Security

This menu tab is used for configuration of user and administrator passwords for access to BIOS Setup.

Fig. 3-18: Screen of "Security" menu

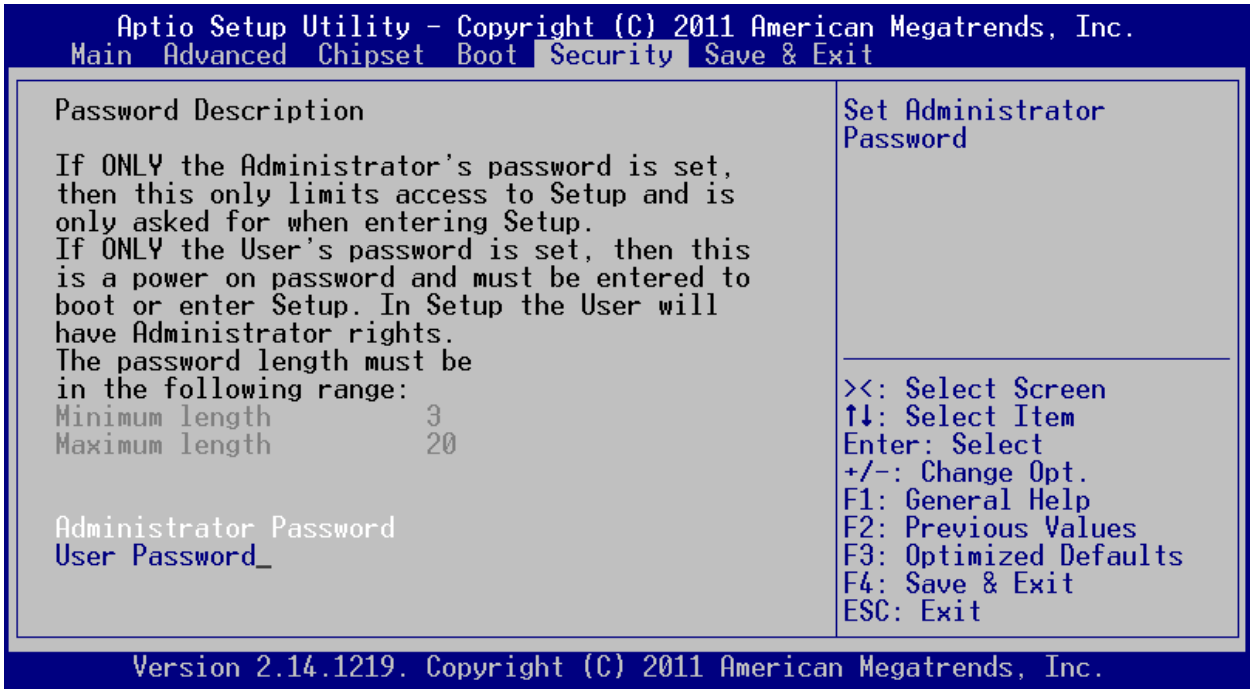


Table 3-16: Description of "Security" menu

Menu item	Description
Setup Prompt Timeout	Timeout for striking the key for entering BIOS Setup
Administrator Password	Administrator Password – for access to all configuration items
User Password	User Password – for access with limited configuration rights

Save & Exit

This menu tab is used for saving or discarding all changes made.

Fig. 3-19: Screen of "Save & Exit" menu

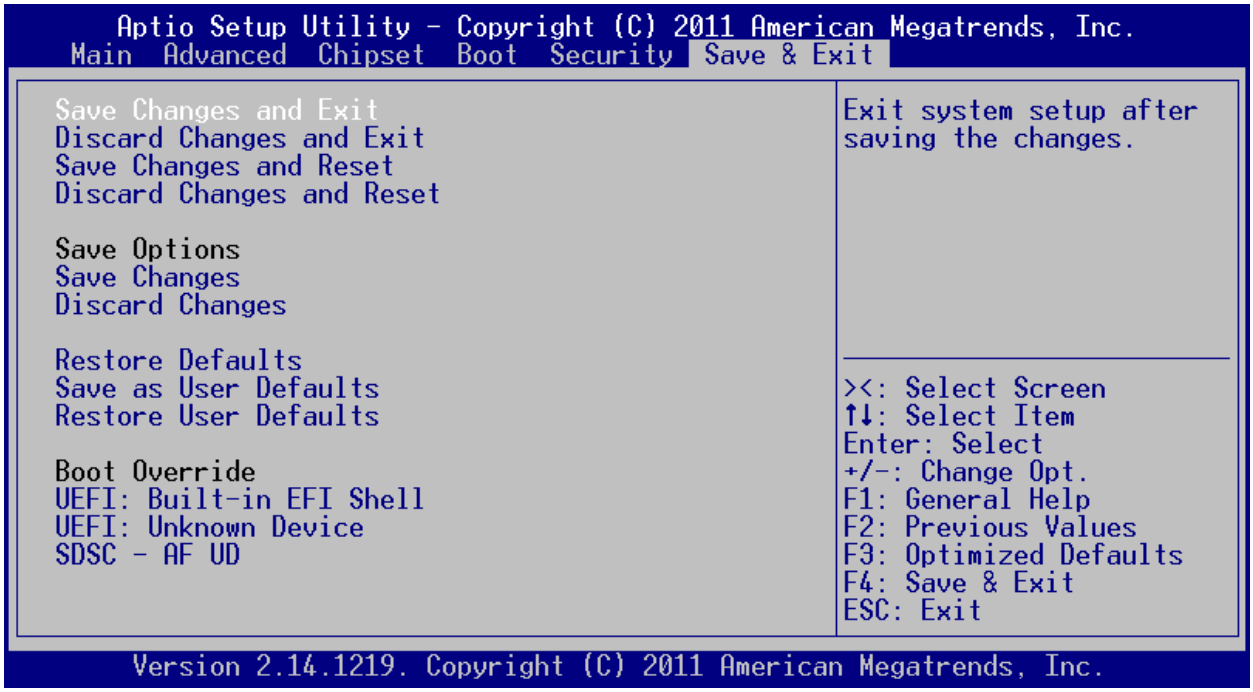


Table 3-17: Description of "Save & Exit" menu

Menu item	Description
Save Changes and Exit	Save carried out changes made and exit
Discard Changes and Exit	Discard carried out changes and exit
Save Changes and Reset	Save carried out changes and exit with reset
Discard Changes and Reset	Discard carried out changes and exit with reset
Save Changes	Save Changes
Discard Changes	Discard Changes
Restore Defaults	Restore default settings
Boot Override	Temporary boot override – boot from the selected device

3.3. Basic software

When delivered, the integrated SSD of CPB907-01 module contains programs, ensuring device readiness for operation:
- integrated FreeDOS operating system, compatible with MS-DOS 6.22;
- system utility for transfer of system signals (sys.com).

Latest versions of documents, BIOS and utilities can be downloaded at:
ftp://ftp.prosoft.ru/pub/Hardware/Fastwel/

3.4. Service programs

3.4.1 SPIFLASH.EXE utility

Spiflash.exe program is designed for modifying BIOS with writing to the SPI-Flash microchip within the CPB907 module.
For modifying BIOS it is required to start the program with "u" key and as a parameter specify BIOS file name:
spiflash u bios.rom

** The utility is under development*

ANNEXES

A. Terms and abbreviations

Term	Meaning
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
AGTL	Advanced Gunning Transceiver Logic
BIOS	Basic Input-Output System
BMC	Baseboard Management Controller
CRT-display	Cathode Ray Tube Display
DAC	Digital-Analog Converter
DDR SDRAM	Double Data Rate Synchronous Dynamic Random Access Memory
DMA	Direct Memory Access
DMI	Direct Media Interface
DVMT	Dynamic Video Memory Technology
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface (Universal Serial Bus specification)
EIDE	Enhanced Integrated Drive Electronics
EOS	Electrical Overstress
ESD	Electrostatically Sensitive Device Electrostatic Discharge
FSB	Frequency System Bus
FWH	Firmware Hub
GMCH	Graphics and Memory Controller Hub
I2C™	Inter Intergrated Circuit
LCD	Liquid crystal display
LPC	Low Pin Count
LVDS	Low Voltage Differential Signal
MDI	Media Dependent Interface
PC	Personal Computer
PIO	Programmed Input/Output
PLCC	Plastic Leaded Chip Carrier
PM	Peripheral Management Controller
POST	Power On Self Test
PSB	Processor System Bus
PWM output	Pulse-Width Modulation
RAMDAC	Random Access Memory Digital-to-Analog Converter
RTC	Real Time Clock
SMB	System Management Bus
SMBus	System Management Bus
SODIMM	Small Outline Dual In-Line Memory Module
SoM	System on a module
SSD	Solid State Disk
TFT	Thin Film Transistor
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver-Transmitter
UHCI	Universal Host Controller Interface
USB	Universal Serial Bus
UTP	Unshielded Twisted Pair